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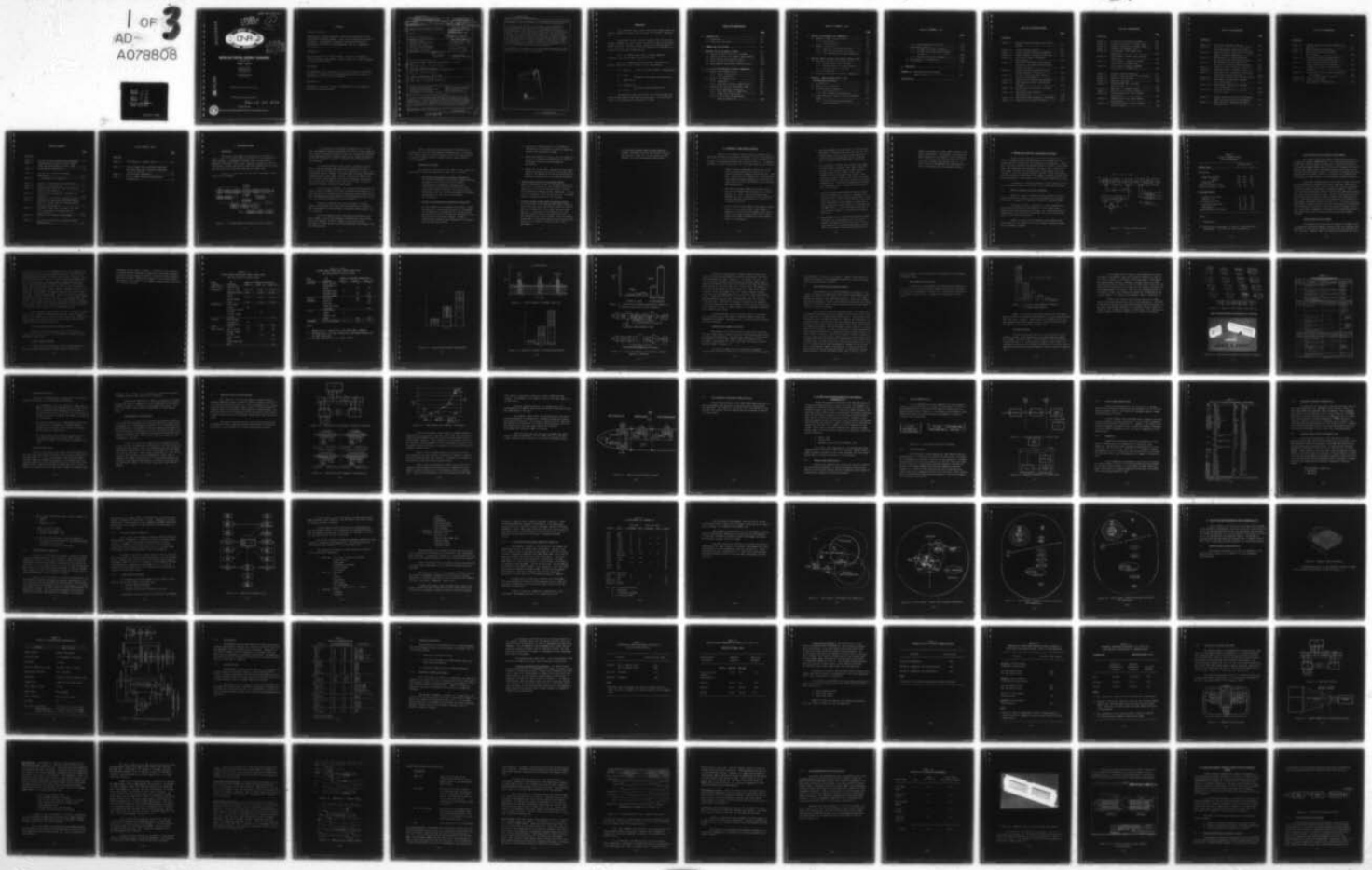


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REPORT ONR-CR233-052-4

LEVEL II

MODULAR DIGITAL MISSILE GUIDANCE

PHASE IV REPORT

FRANK J. LANGLEY

Raytheon Company
Missile Systems Division
Bedford Mass 01730

Contract N00014-75-C-0549
ONR Task 233-052

Technical Report for Period 1 JAN 77 - 31 DEC 77

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A set of macromodular microcomputer specifications has been prepared to meet a wide range of missile guidance and control requirements. These specifications define the function performance and interface requirements of each microcomputer module i.e. microprocessor, memory and input-output I/O interface for analog and serial digital I/O, such that device technology →over

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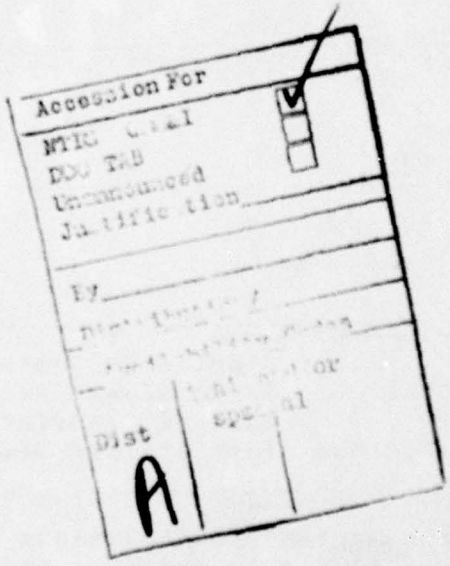
improvements can continually be accommodated within the bounds of module function performance and interface requirements.

To ensure such flexibility in design, other alternative device technologies were reviewed and evaluated for the MIL-STD-4553A serial digital I/O interface and the spectrum analyzer module, viz: fiber-optic data link and charge-coupled device, (CCD), very-large-scale integration (VLSI) analyzer options. In addition the requirements for universal microcomputer development systems were explored in order to support both medium-speed single-chip microprocessors and high-speed bit-slice emulators to preserve software commonality. Lastly, the compatibility of the Navy AN/UYK-30 microprocessor with the macromodular microcomputer family was investigated on the basis of throughput and electrical interface.

In summary, this phase of the program has culminated in the generation of a practical set of microcomputer module specifications for multi-source procurement.



PREFACE

This technical report covers the work performed under Contract No. N00014-75-C-0549 from 1 January 1977 through 31 December 1977.

The purpose of this contract together with the work performed in Phases I, II and III was to provide a basis for designing modular air-to-air missile guidance systems with improved performance, flexibility and growth features compared to traditional analog and early digital implementations.

Cdr. L. E. McCullough, Office of Naval Research, Arlington, Va., was the Navy Scientific Officer.

Mr. F. J. Langley was the Principal Investigator for Raytheon supported by the following study team members:

A. J. Mannion	8 and 16-Bit Microcomputer Commonalities
K. D. Laube J. Demetrick	AN/UYK-30 Peformance and Commonality
D. S. Goldstein A. J. Mannion	CCD FFT Module Mechanizations

Publication of this report does not constitute Navy approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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1. INTRODUCTION

1.1 Background

The design, development and production of missiles to cover a range of presently defined missions with the capability of being upgraded to accommodate changing threat situations and advancing technology without major redesign, stresses the need for more modular guidance and control electronics possessing both physical and electrical flexibility features at lowest cost.

Figure 1.1 illustrates the functional complement typical of air to air missiles.

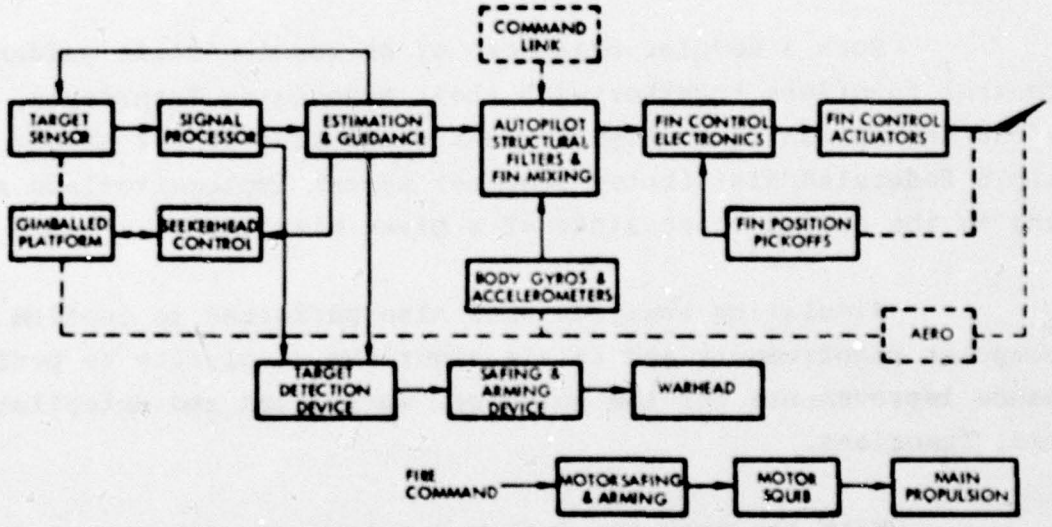


Figure 1.1 - On-Board Missile Guidance and Control System

In the previous study phases (References R-1, R-2 and R-4), programmable digital techniques were shown to offer improved performance and greater flexibility than the traditional hardwired analog implementations of seeker head control, signal processing, estimation, guidance, autopilot, warhead fuzing, telemetry and test functions.

To achieve modularity and growth in hardware and software, a top-down system study approach was adopted, by first dividing the entire range of air to air missiles into a set of distinguishable generic classes, including upper and lower performance boundaries within each class, then by: defining the major functions and data rates amenable to digital processing, determining their constituent software modules and sizing these in terms of computer throughput and memory requirements.

Such a modular breakdown of on-board missile guidance and control functions together with their associated interfaces, provided the option of configuring and evaluating either single or multiple federated/distributed computer system implementations according to the design constraints of a given missile.

Simulation analyses were also performed to confirm computer requirements and relate algorithm complexity to performance improvements for the guidance, estimation and autopilot/ control functions.

With the computer design requirements determined from these studies, a set of microcomputer "macromodules" was defined which would support the entire range of air-to-air missile functions, in either single or multiple/federated microcomputer system configurations.

Lastly, the modules were simulated individually and collectively, as whole microcomputer configurations, to validate their effectiveness in missile guidance and control applications to the point where realistic product function specifications could be prepared.

1.2 Objectives and Scope

The objectives and scope of the Phase IV study under the modification of contract N00014-75-C-0549, are as follows:

1. 8 and 16-Bit Microcomputer Software Commonality
   To obviate the need for two distinct support software packages for the 8 and 16-bit microcomputer configurations, commonality features will be identified in the areas of instruction sets and associated mnemonics together with common system development aids e.g. Intel microcomputer development system (MDS) for the 8080 and 3000 series microprocessors.

2. NA/UYK-30 Performance and Commonality Evaluation

   The Navy AN/UYK-30 microcomputer has become a viable alternative to the limited emulation of the AN/UYK-20 and AN/AYK-14 minicomputers for digital missile applications, therefore warranting the pursuit of the following study sub-tasks, namely: AN/UYK-30 architecture, interface and packaging review based on data furnished by the Navy.

a. Evaluate the effectiveness of the AN/UYK-30 architecture in executing a steering command generation loop bench-mark program.

b. Review the AN/UYK-30 microbus and its compatibility with the ONR macro modules both in terms of electrical interface and microcomputer performance.

c. Review the current Navy standard avionics module (SAM) and standard electronic module (SEM) packaging of the AN/UYK-30 and the corresponding compatibility implications of the ONR macromodules.

3. Low-Cost Serial Digital Input-Output Module

Explore alternative serial I/O interface designs for use within the missile as a more simple, low-cost alternative to the avionics MIL-STD-1553A interface while maintaining message format commonality. In particular investigate fiber-optics data link techniques Define a feasible module for this purpose.

4. Low-Cost Charge-Coupled Spectrum Analyzer Module

As an alternate to the digital μFFT module, define a module with equivalent performance using CCD technology and interfacing with the radar receiver and/or ONR μbus. Investigate the incorporation of pre-spectral analysis signal processing functions, i.e. $\cos^2$ weighting and corner-turning, within the module. Define what is a practical design using existing technology and the impact of future trends in CCD development.

5. Critical Item Product Function Specifications

Prepare individual Critical Item Product Function Specifications Type C2a, in accordance with MIL-STD-490, for each microcomputer macromodule.

2. SUMMARY AND CONCLUSIONS

Phase IV of the Modular Digital Missile Guidance Study performed the additional analysis necessary to ensure the specification of a set of microcomputer macromodules which are sensitive to a number of technology-related cost reduction factors. In summary, the major findings and products of this study phase are as follows:

1. Common software development systems for 8 and 16-bit microprocessors are feasible and are planned by several commercial manufacturers. However, instruction set commonality is non-existent and assembly language commonality is minimal between 8 and 16-bit microprocessors, even from the same manufacturer.

2. High-order language commonality between 8-bit, and 16-bit microprocessors exists to a certain degree, viz: PL/1 - derived languages and FORTRAN, but their languages are not totally machine-independent, particularly in terms of arithmetic precision.

3. A "full-service" microcomputer development system (MDS), i.e. one which offers a HOL Compiler, Assembler and microcode development aids, would support both medium-speed single-chip microprocessors and higher-throughput bit-slice equivalents (i.e. emulators).

4. The Navy AN/UYK-30 microprocessor could be easily modified to interface with the μBus, and its performance meets the throughput requirements for missile steering command generation, although this is significantly slower than a PDP-11/34.

5. The transformer-coupled serial digital multiplexed input-output interface, specified in MIL-STD-1553A, is out of place within a small missile. Low-performance (DC to 2Mb/s) fiber-optic couplers offer significant size, weight, power and cost savings. However, the lack of low-loss T-couplers inhibits the use of a party-line inter-subsystem bus. Alternative communication schemes are roundrobin ring or centrally controlled radial star systems.

6. Current Schottky-bipolar FFT processors require over 150 SSI/MSI/LSI circuits to implement and therefore dwarf single-chip microprocessors. Analog chirp Z transform (CZT)CCD devices, currently under development, show promise of achieving a 2-chip spectrum analyser module to interface with the ADAC module. A two-chip digital CCD FFT is also feesible subject to a significant development effort.

7. MIL-STD-490 Critical Item Product Function Specifications for an optimum set of eight microcomputer macromodules are contained in this report based upon the analysis performed to date. Their microcomputer module specifications will

support the needs of a wide range of missile computer requirements. Furthermore, they allow complete freedom for the supplier to be innovative in the design provided that the form, fit, function and interface requirements are met. As such, they will accommodate the improvements in device technology when they become available.

3. MODULAR DIGITAL GUIDANCE SYSTEMS

Recent studies have shown that the performance and flexibility of onboard missile guidance and control systems can be greatly improved through the use of modular microcomputers. Based upon functional analyses and system simulation results, 14 microcomputer "macromodules" were defined to satisfy a wide range of missile types, form factors and performance requirements, from the simplest to the most complex guidance systems. These macromodules utilize existing microprocessors and support software together with associated memory, input-output and high-speed arithmetic circuits.

In support of the above findings a brief overview of the work performed to date will be given in the following paragraphs.

3.1 Missile Guidance and Control Systems

Figure 3.1 shows a typical missile guidance and control system divided into the major functional elements with switches indicating the sampling or updating of data in a digital sense.

Three major control loops exist in such a system two of which perform body motion stabilization of the target seeker gimballed platform and missile airframe, i.e., head and autopilot respectively, and the third loop the generation of steering commands to the head and autopilot.

Table 3.1 lists the corresponding data sampling and update rates for the range of air-to-air missile systems divided into three major classes.

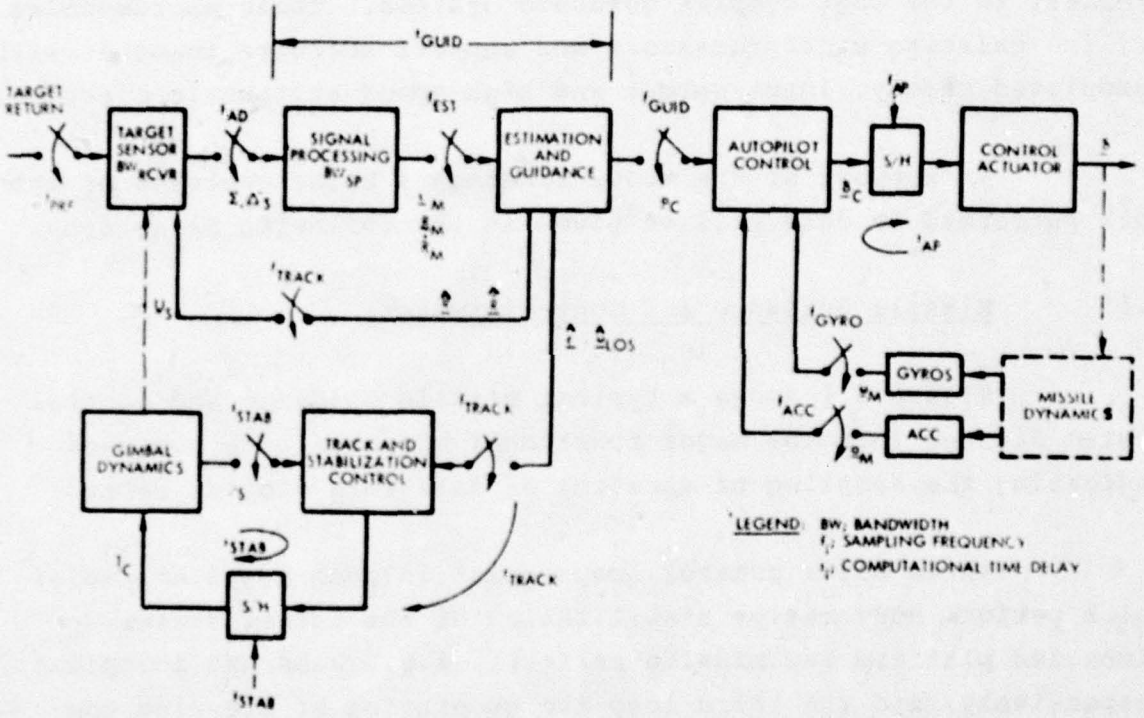


Figure 3.1 - Digital Guidance System

TABLE 3.1

DIGITAL GUIDANCE SYSTEM

DESIGN PARAMETERS

CONTROL LOOP	MISSILE CLASS I	II	III
Body Motion			
$f_{STAB}/f_{AP}/f_{GYRO}$(Hz)	250	500	500
f_{ACC}(Hz)	125	250	250
f_{STAB}/t_{AP}(μs)	800	600	600
A-D/D-A Conversion (bits)	10	12	12
Computing Precision (bits)*	16	16	16
Steering/Guidance			
f_{AD}Acquisition (KHz)	25	128	256
f_{AD}Track (KHz)	20	32	32
A-D Conversion (bits)	8	10	10
$f_{EST}/f_{GUID}/TRACK$ (Hz)	20	30	40
t_{GUID}(msec)	40	30	20
Computing Precision (bits)**	16	8-16	8-16

Legend

* Fixed-point

** Floating-point mantissa. 8 bits for covariance-matrix propagation. 12-16 bits for state propagation.

3.2 Digital Functions and Computer Requirements

The primary ground rule used in determining functions suitable for digital implementation, was "improved performance and flexibility without severe cost penalty". Functions selected on this basis encompass almost the entire missile guidance and control system, from target sensor base band frequency interfaces to missile fin control actuator drivers. Functions so selected were then analyzed and algorithms written for conversion into computer program modules for use as part of a hierarchical program structure.

Individual program modules were sized in terms of the number of add/subtract, multiply/divide and load/store instructions involved in the worst-case, time critical path through the module, to form the basis of worst-case throughput estimates. Table 3.2 lists the selected digital missile functions and associated instruction counts for each missile class. Function sophistication grows across the range of missile classes together with computational cost. Total module instruction counts determine the computer program memory requirements given in Figure 3.2. To account for program module linkages, scaling and other miscellaneous overhead operations necessary to achieve a fully operational program, instruction counts were increased by 30 percent short-type orders based on experience with current in-house digital missile development programs.

System Timing and Throughput

To determine the worst-case GP computer throughput rates for federated and single computer systems, time line analyses were performed to identify worst-case function mixes and computational time intervals. Mission time line analyses showed that the worst-

case function mix (i.e., full complement) for single computer systems occurred in the Terminal/Target Track Mode. Further fine timing analyses revealed a critical time interval (T_{CRIT}) of 30, 20 and 10 ms duration for Class I, II and III missiles, respectively. During this interval, steering/guidance command loop functions (i.e., signal processing, estimation and guidance), and target seeker and airframe stabilization and control functions would require time multiplexing in single computer systems, (Figure 3.3) as opposed to the assignment of separate computers to each of these functions in federated approaches. Figure 3.4 shows the resulting throughputs for each missile class both in totum for single computer systems, and by major function for distributed computer applications. Signal processing throughput requirements apply to postspectrum analysis, (FFT), radar data processing and can vary according to the dwell time and size of the range/Doppler matrix.

FFT throughput requirements are shown in Figure 3.5 based upon 64-point complex transform execution rate, since 64 points tend to be a common size in missile signal processing. Compared to existing ground air defense and avionics processor capabilities, missile FFT requirements are modest.

Single and Federated Microcomputer Systems

Figure 3.6 shows the missile system configurations resulting from single central and federated microcomputer design approaches respectively.

Single Computer Systems

Single computer guidance and control systems require a multiwire analog and digital interface between all missile

subsystems and the central computer. Similarly in the software, all program modules required to support the individual hardware subsystems must be time-multiplexed to maintain the data sampling rates and allowable computational delays for the various control loops which in turn results in a complex software module interface, i.e., program linkages.

TABLE 3.2

PROGRAM MODULE OPERATIONS COUNTS (WORST-CASE)

AND APPLICATION BY MISSILE CLASS

MAJOR FUNCTION	SUB FUNCTION	NUMBER OF COMPUTER OPERATIONS(*) CLASS I	CLASS II	CLASS III
RADAR SIGNAL PROCESSING	ACQUISITION			
	FFT(**) +PDI	6,910 (1)	36,160 (5)	72,300 (10)
	DETECTION LOGIC	1,200	6,900	16,200
	TRACK			
	FFT(**)	18,240 (3)	30,400 (5)	30,400 (5)
	ERROR GENERATION	1,330	1,370	1,370
ESTIMATION	FIXED GAIN FILTER	160	-	-
	DECOUPLED KALMAN FILTER	-	250	-
	COUPLED KALMAN FILTER	-	-	375
GUIDANCE	PROPORTIONAL NAVIGATION	40	-	-
	AUGMENTED PN	-	240	240
SEEKER STABILIZATION	AIMING	10	10	10
	BASIC CONTROL	100	100	100
	RADOME COMPENSATION	-	340	340
	GYRO & TORQUE COMP.	-	-	110
	NINE-STATE FEEDBACK	-	-	195

TABLE 3.2 (CONT.)

PROGRAM MODULE OPERATIONS COUNTS (WORST-CASE)

AND APPLICATION BY MISSILE CLASS

MAJOR FUNCTION	SUB FUNCTION	NUMBER OF COMPUTER OPERATIONS(*) CLASS I	CLASS II	CLASS III
AUTOPILOT	BASIC CONTROL	80	80	80
	STRUCTURAL FILTERING	-	105	105
	SWITCHED GAINS	20	-	-
	VARIABLE GAINS	-	490	490
	AERO ESTIMATES	-	-	2,765
INERTIAL REFERENCE	ATTITUDE	-	300	300
	VELOCITY	-	130	130
	POSITION	-	-	100
	ANGLE OF ATTACK & BALANCE	-	-	130
FUZING	SIMPLE TIME DELAY	15	-	-
	COMPLEX TIME DELAY	-	350	350
TELEMETRY	NO. OF VARIABLES	30	40	50

NOTES:

( ) NUMBER OF 64 PT. COMPLEX FFT'S PER RADAR DWELL INTERVAL.

(*) PER RADAR DWELL FOR SIGNAL PROCESSING; PER UPDATE INTERVAL FOR ALL OTHER FUNCTIONS.

(**) INCLUDES TIME-WEIGHTING AND CORNER-TURNING.

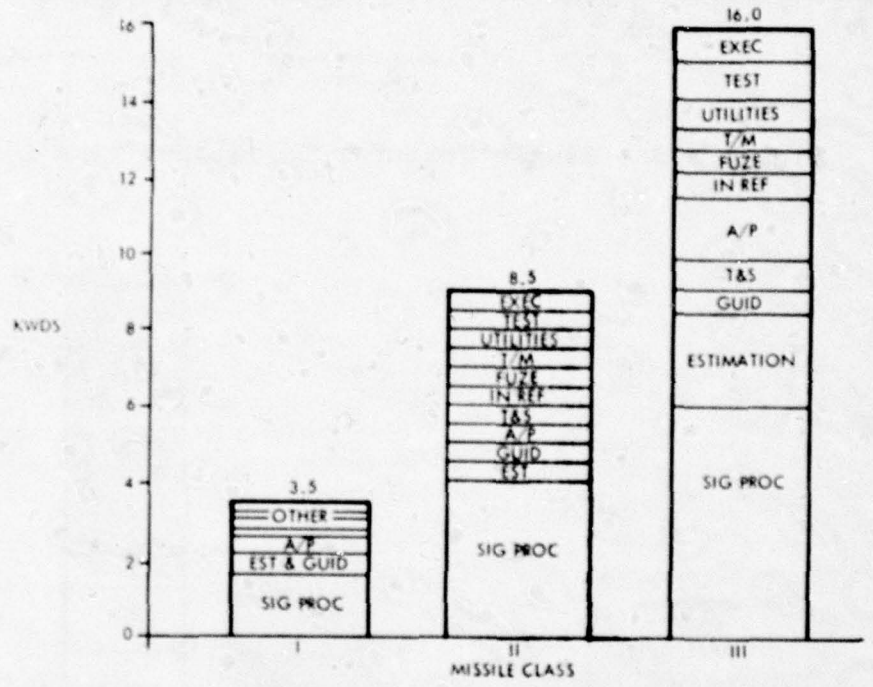


Figure 3.2 - Digital Missile Memory Requirements

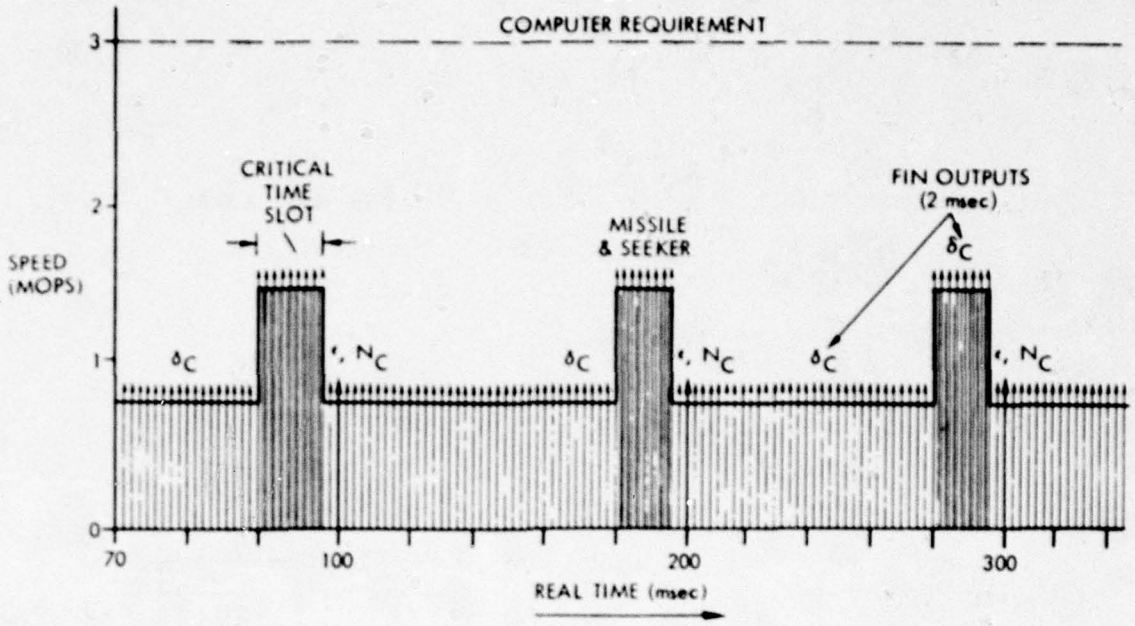


Figure 3.3 - Single Computer Throughput Time Line

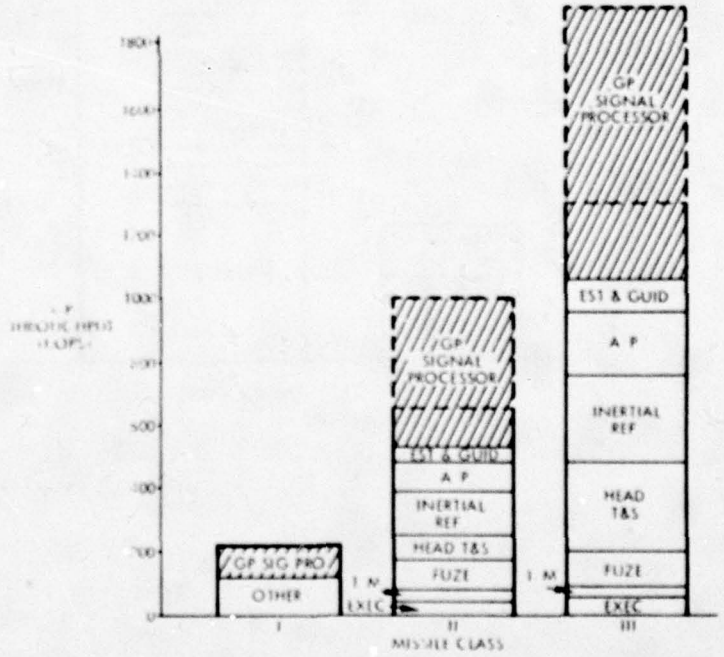


Figure 3.4 - Missile GP Computer Throughput Requirements

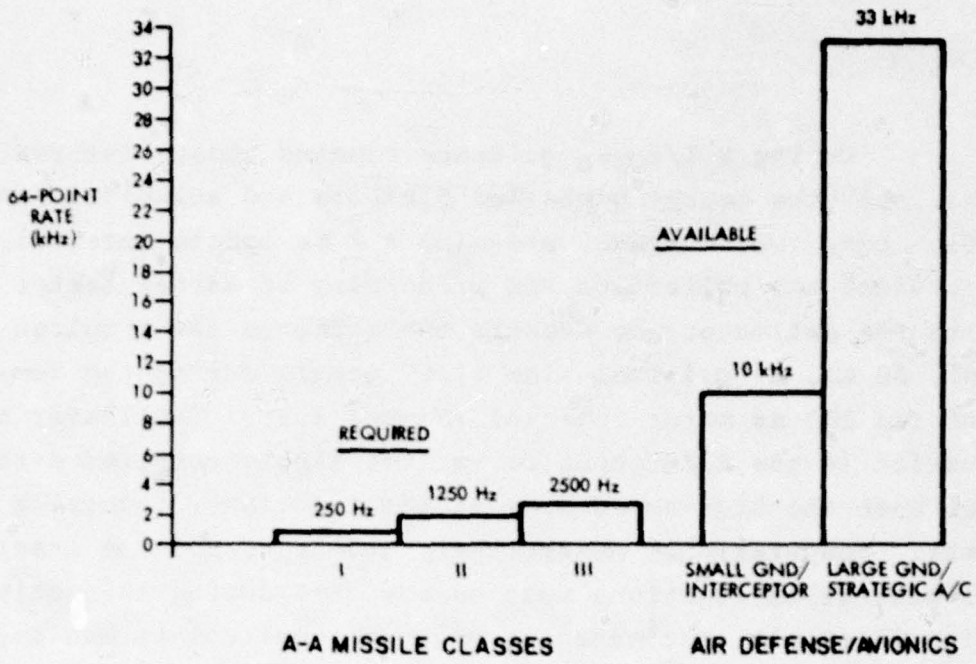
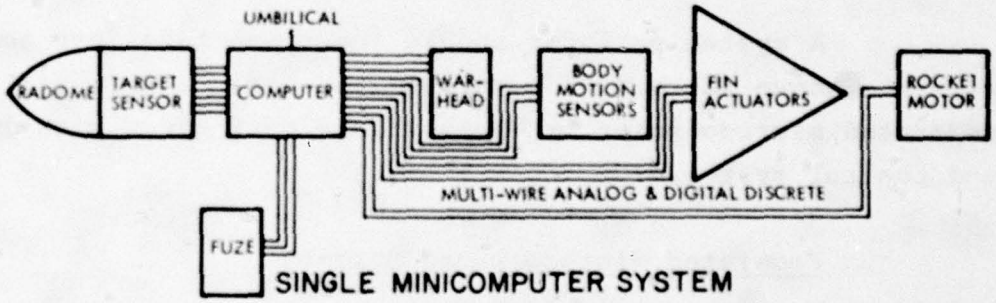


Figure 3.5 - Missile FFT Throughput Requirements Compared to Air Defense and Avionic Signal Processors



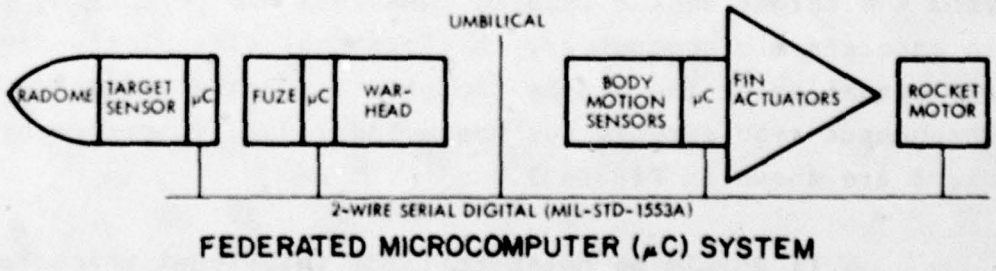


Figure 3.6 - Single and Federated Microcomputer Systems Applied to Missiles

During a $1/f_{GUID}$ guidance command update interval say, 100ms, both the seeker gimballed platform and autopilot functions must be computed 50 times, assuming a 2 ms update interval. Further, since the collection and processing of target seeker data to update the estimator and execute the guidance law requires approximately 80 ms, a "critical time slot" occurs during the remaining 20 ms of the 100 ms major interval (Figure 3.3). The latter timing situation is the throughput driver for single computer systems, since both the high-speed body motion functions, requiring 600-800 μs max. Computational delay (t_{STAB} and t_{AP}), and the steering command generation functions must be computed during this critical timing interval. Estimated throughput requirements can approach 1.5 million operations per second (MOPS), which, with a 100 percent safety margin, requires a 3 MOPS computer to accommodate estimating errors and possible growth.

A system designer should therefore take into consideration the above factors when making tradeoffs between single and federated microcomputer implementations of a given missile guidance and control system.

Federated Microcomputer Systems

By separating out the body motion stabilizing functions from the target seeker related functions and performing these tasks in separate microcomputers, the "critical time slot", high throughput situation of the single computer case is eliminated. The throughput requirements for these individual functions by missile class are shown in Figure 3.7

It should be noted that the individual throughputs required fall within the capability of conventional general-purpose

microcomputers currently on the market. Memory requirements are similarly reduced to more manageable proportions from a software design and development viewpoint.

3.3 Macro Modular Microcomputer Family

The available mini and microcomputers evaluated in the context of missile guidance and control system requirements, while capable of supporting the respective computer loads, lack common modularity features, and, even more important, they lack a common programming language. These two deficiencies constitute major drawbacks for low-cost, modular growth, design flexibility and simple logistics in missile systems.

The solution to the first problem lies in the definition of standard, major/macrofunction computer modules each with a standard interface to a common interconnecting bus. Such minimal standardization would provide the means of changing the performance of a given computer configuration by interchanging memory modules with different cycle times, central processing units (CPUs) with different computing features, and input-output channel types to suit the specific I/O situation, in order to achieve the desired performance and programming features for a specific missile computing task. In other words, to achieve a best-fit of computer hardware configuration at lowest-cost and without restrictions on future growth to accommodate changing technology both in performance and circuit packing densities. An ideal solution to the second problem lies in the use of a common higher-order programming language for all processors in the computer family, and moreover, a language which supports modular structured program design. As a practical interim measure however, proven and widely-used support software of an

existing computer offers significant cost savings in the software development cycle.

Microcomputer Macromodules

A total of 14 microcomputer macromodules were defined to cover the entire range of missile guidance and control processing and interface requirements. Figure 3.8 is a pictorial illustration of the module types and their respective interfacing characteristics.

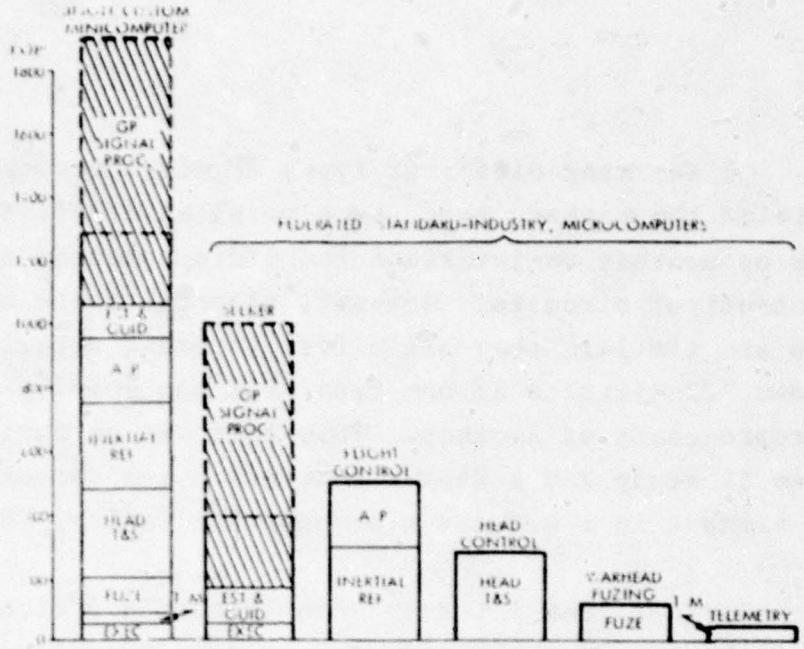


Figure 3.7 - Central versus Federated Computer Throughput Requirements

Table 3.3 lists the significant features of each macromodule and their corresponding applications in digital missile guidance and control systems. These modules are compatible with the Navy standard electronic module plug-in circuit boards in either the SEM-1A or 2A configuration, (Figure 3.9).

Standard Microbus

The most significant factor in the macromodular microcomputer concept is the definition of a common parallel digital bus, termed a microbus (μBus), which enables various combinations of macromodules, i.e., microprocessor, memory, input-output and high-speed arithmetic, to be readily combined to form a whole microcomputer having the desired performance to match a specific application.

Of the many different types of microcomputers currently available on the market, most use a parallel digital bus (ses) of one form or another to interface the microprocessor to the memory and input-output circuits. However, although these bus configurations are similar, they all differ in small detail such that the memory and I/O circuits of one type will not readily interface with the microprocessor of another. This fact was recognized early in the Phase II study and a standard microbus was recommended as the crucial element in a modular microcomputer family, (Reference 2).

Further, the internal architecture and circuit composition of the macromodules can vary to take advantage of new technology and innovative cost-saving/performance improving designs, as and when these become available, on a module-by-module basis provided that the standard interface is maintained. This obviates the need to redesign the whole computer as is currently customary.

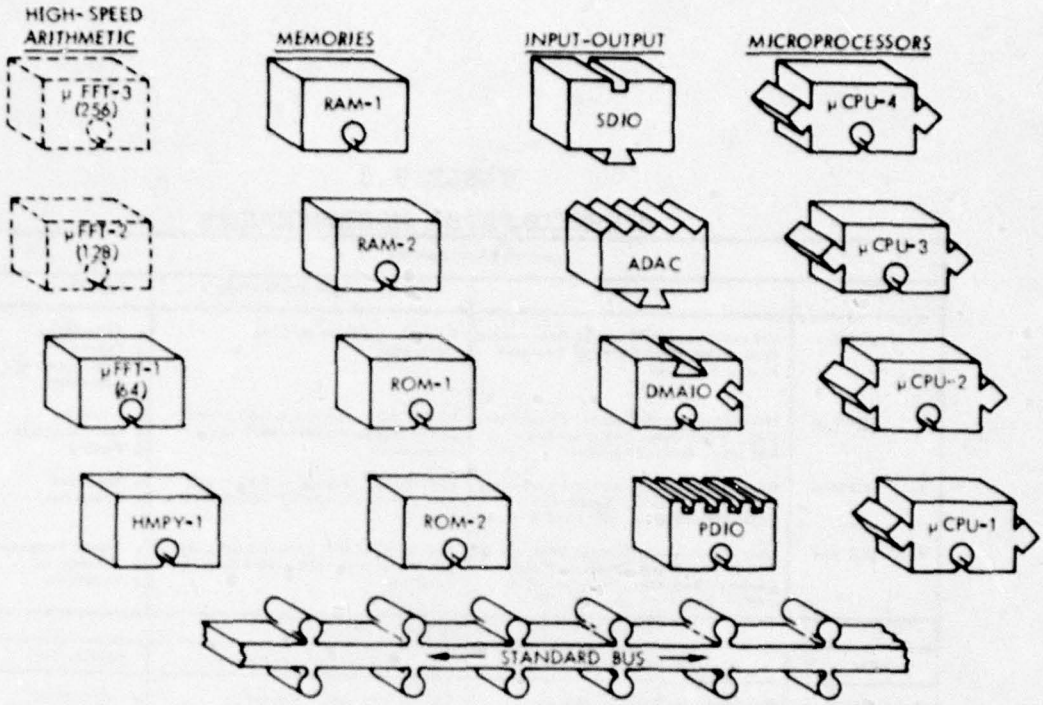


Figure 3.8 - Family of Microcomputer Macromodules

NAVY SEM MICROCOMPUTER MACROMODULE PACKAGING

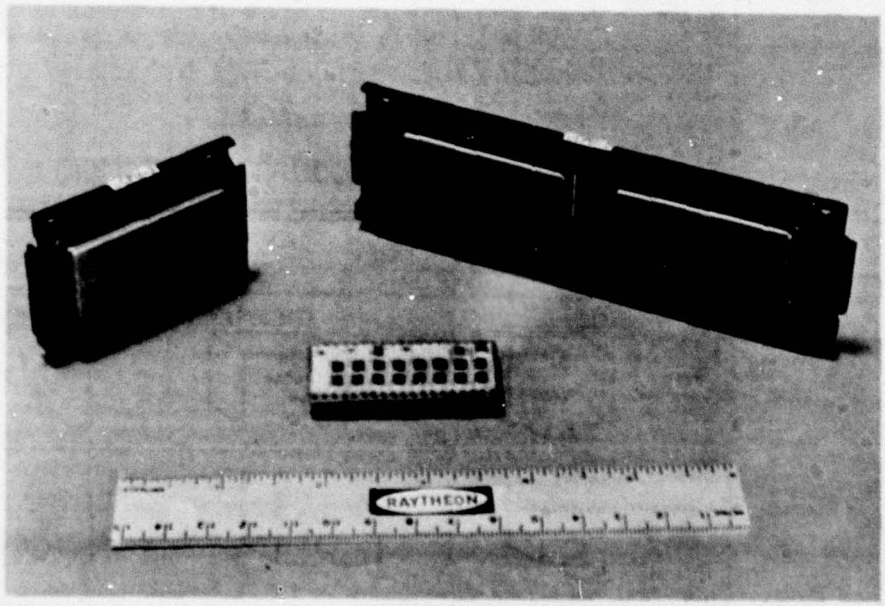


Figure 3.9 - Navy SEM Microcomputer Macromodule Packaging

TABLE 3.3

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

SEM	Description	VSLI Circuit Technology	Application
1. μCPU-1	Microprocessor/Central Processing Unit, 8-bit Byte General Register 2 μsec R-R Add	N-MOS, CPU-on-a-Chip, (MIL 8080)	• Telemetry • Fuzing • Head Control • Autopilot
2. μCPU-2	Microprocessor/Central Processing Unit, 8-bit Byte, General Register 600 nsec (8080 Emulator)	CMOS-SOS, Bit-Slice RALU and μPCU Hybrids (2900/3000 Series or Equiv.)	• Autopilot • Head Control • Fuzing
3. μCPU-3	Microprocessor/Central Processing Unit, 16-bit Word, Fixed-Point, General-Register, 600 nsec R-R Add	CMOS-SOS, Bit-Slice RALU and μPCU Hybrids (2900/3000 Series or Equiv.)	• Autopilot (Adaptive)
4. μCPU-4	Microprocessor/Central Unit, 16-bit Word, Fixed and Floating-Point, General-Register, 600 nsec R-R Add (1.0 to 3.25 μsec Flt. Pt.)	CMOS-SOS, Bit-Slice RALU and μPCU Hybrids (2900/3000 Series or Equiv.)	• Signal Processing • Estimation • Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

SEM	Description	VSLI Circuit Technology	Application
5. HMPY-1	Hardware Multiplier, 200 nsec, 16 x 16-bit Multiply	CMOS-SOS Single Hybrid	• Throughput Enhancement for μCPU F, G, Class I Sig. Proc.
6. μFFT-1	Micro Fast Fourier Transform Processor, 40-400 μsec 64-pt. 8 x 2k	CMOS-SOS or CCD RALU and μPCU Hybrids (2900 Series or Equiv.)	• Throughput Enhancement for μCPUs F, G, Class II and III Sig. Proc.
7. RAM-1	Random-Access, Read/Write Memory, Medium-Speed, 128-2K Bytes 500 nsec Max. Access Time	N-MOS DIP/Hybrid	Data: • Telemetry • Fuzing • Head Control • Autopilot
8. P/ROM-1	Programmable (Mask/Electrically) Read-Only Memory, Medium-Speed, 1K-16K Bytes, 500 nsec Max. Access Time	N-MOS DIP/Hybrid	Programs: • Telemetry • Fuzing • Head Control • Autopilot
9. RAM-2	Random-Access, Read/Write Memory, High-Speed, 256-1K x 16-bit or 256-2K Bytes, 100 nsec Max. Access Time	CMOS-SOS DIP/Hybrid	Data: • Sig. Proc. • Estimation • Guidance • Head Control • Autopilot • Fuzing
10. P/ROM-2	Programmable (Mask/Electrically) Read-Only Memory, High-Speed, 1K-4K x 16-bits or 1K-8K Bytes, 100 nsec Max. Access Time	CMOS/SOS DIP/Hybrid	Programs: • Sig. Proc. • Estimation • Guidance • Head Control • Autopilot • Fuzing

INPUT - OUTPUT

SEM	Description	VSLI Circuit Technology	Application
11. DMA10	Direct Memory Access Input-Output Channel, Parallel Word/Byte Transfers to/from Microcomputer RAM	CMOS-SOS/Bipolar Single Hybrid	All Microprocessor Applications
12. PD10	Parallel Digital Input-Output Channel Parallel Discrete Transfers to/from μCPU	CMOS-SOS/Bipolar Single Hybrid	• Telemetry
13. ADAC	Analog to Digital/Digital to Analog Input-Output Channel A-D: 8/16/24 Chs., Sim, S/H, Mux 8/10/12-Bit, A-D 3/6/8 μsec Max/Ch. D-A: 8 Chs. Demux., S/H, 12-bit D-A, 4 μsec Max/Ch.	CMOS-SOS Single Hybrid	• Head Control • Autopilot • Telemetry • Radar Receiver
14. SDI10	Serial Digital Input-Output Channel Word and Bit Serial Data/Command Transfers, 1Mbit/sec Max, MIL-STD-1553A	CMOS-SOS Single Hybrid	• Avionics • Inter Microcomputer

μBus Design Rationale.

The use of a standard μBus is based upon a high degree of functional autonomy in the interfacing macromodules.

1. All macromodules, with the exception of RAMs and (P) ROMs, incorporate microprogram control to perform the various operating mode sequences and interface responses without action on the part of the μCPU and operational software, excepting the simple initializing of the modules.

2. To minimize overhead (e.g., LOAD/STORE) instructions, optimize useful throughput and reduce frequent access/use of the μBus, each μCPU uses a multiple/general-register architecture.

3. All input-output data transfers are made via a direct-memory-access input-output (DMAIO) module incorporating memory block addressing registers and logic.

μBus Interface Lines.

Since all μBus modules are treated as memory modules by the μCPU a practical memory interface drives the bus configuration. With the advent of 8-bit microprocessors, byte organized semiconductor RAMs and (P)ROMs have appeared on the market, and with these new memory-on-a-chip modules the provision of multiple "chip select" lines. Based upon the above technology trend, the new memory-on-a-chip LSI circuits were used to establish standard μBus

interface lines. Figure 3.10 illustrates the resulting interface arrangement between μCPU, memory and I/O modules.

Adopting the semiconductor memory interface as a standard obviates the need to repackage RAMs and (P)ROMs and allows modular expansion of memory on a dual in-line package (DIP) basis. Further, chip select lines become the equivalent of module select lines.

Microcomputer Configurations

Figure 3.11 shows four different microcomputer configurations using the macromodule building-block approach, ranging from a low-speed 8-bit, 8080A-based configuration to a high-speed 16-bit CMOS-SOS AN/UYK-20 and AN/AYK-14 software compatible microcomputer. These microcomputer configurations can be used either singly, or as a group in federated microcomputer systems using the MIL-STD-1553A compatible serial digital input-output (SDIO) macromodule as the intercomputer interface.

Figure 3.12 plots the respective gp throughputs of each of the four basic microcomputer configurations with and without the hardware multiply module, which are compatible with the throughput requirements determined in the initial study phases for the range of air-to-air missiles. Radar signal processing e.g., fast Fourier transform (FFT) processing is accommodated by either μCPU-3 supported by a HMPY-1 μBus module for low performance semiactive continuous wave (SA-CW) radar seekers, or μCPU-3/-4 and the hardware FFT module (μFFT-1) for multiple range gate, pulse doppler seekers.

3.4 Federated Digital Missile System

As a result of the previous computer system analyses, a feasible federated computer system for missile guidance and control is of the form shown in Figure 3.13. Four microcomputers of varying configurations and performance capabilities, from the macromodular computer family, are matched to the respective, semiautonomous, missile functions which in themselves follow the physical partitioning of major missile functions for design, manufacture, test and maintenance.

The body motion stabilization and control processors are colocated with their respective sensors and actuators and execute the control loop functions in an uninterrupted cyclic manner.

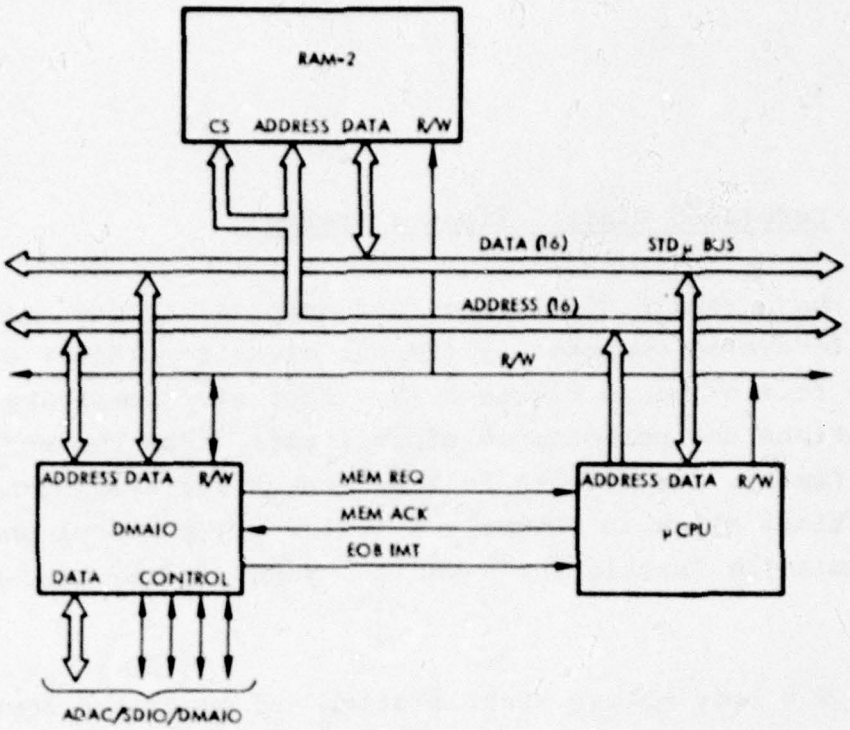


Figure 3.10 - Macromodular Microcomputer Standard Interfaces

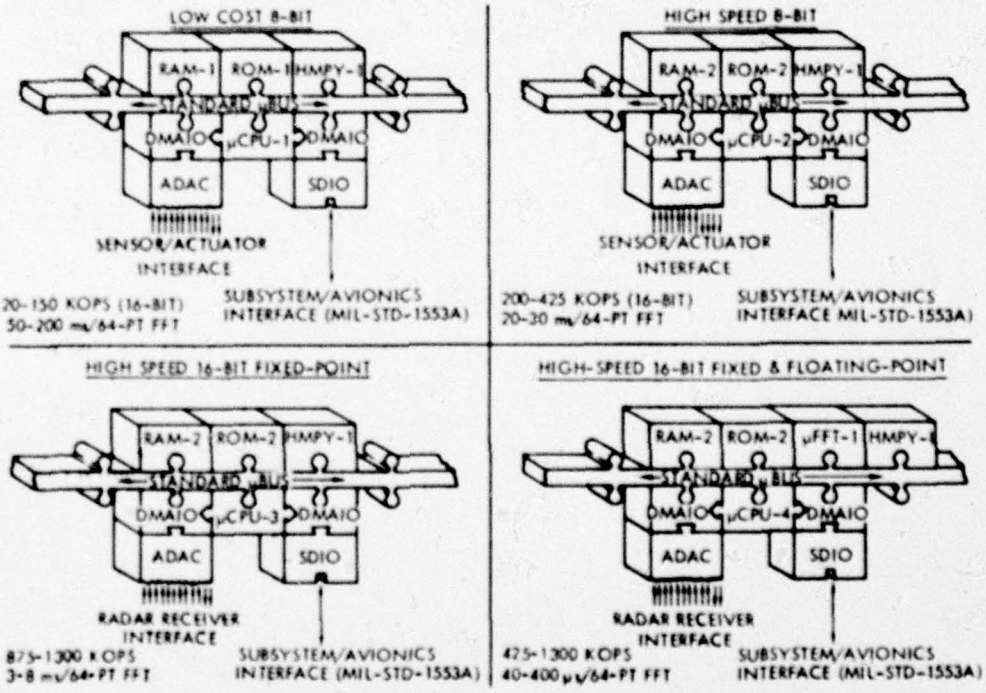


Figure 3.11 - Macromodular Microcomputer Configurations

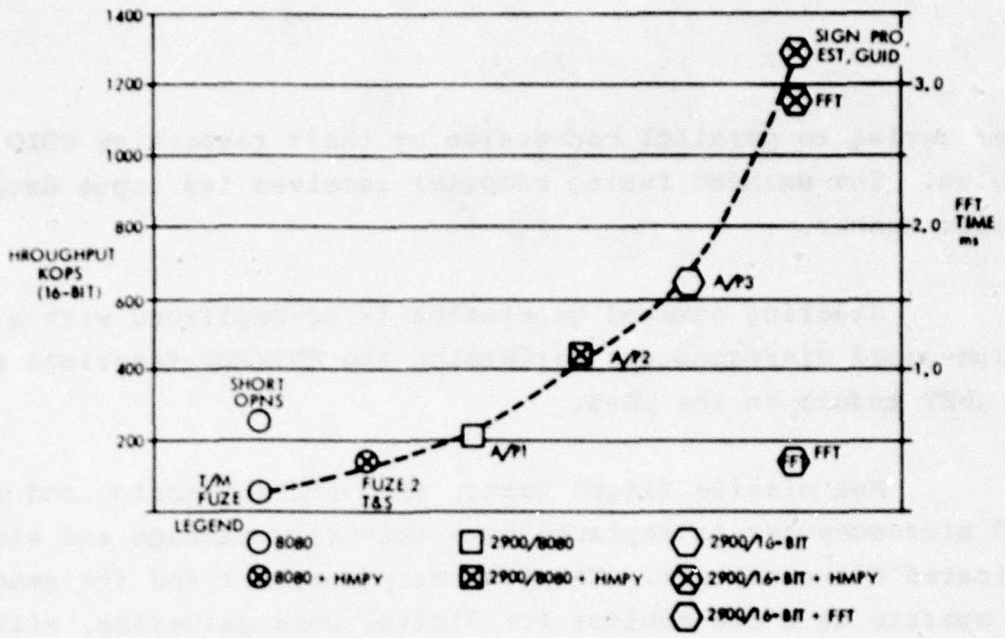


Figure 3.12 - Macromodular Microcomputer Throughputs

A two-wire redundant, serial digital, command/response, multiplex bus, as defined in MIL-STD-1553A, forms the interface between all microcomputers and the carrier aircraft weapon control system (AWCS) computer. This interface is an outcome of the critical evaluation and development of avionics system integration over the past few years through such programs as the Digital Avionics Information System (DAIS).

Before launch the AWCS computer controls the missile microcomputers via a bus control interface unit (BCIU) to subordinate microcomputer SDIO (RTU) modules. (The SDIO of the seeker μC functions as an RTU during the prelaunch mode.)

After launch, the body motion stabilization and control computers receive appropriate steering and g commands from the seeker μC asynchronously at the low-frequency, 10-40 Hz, update-rate. Input of these parameters is by direct-memory-access (DMA)

after serial to parallel conversion by their respective SDIO modules. The warhead fuzing computer receives its input data in a similar manner.

Steering command generation is accomplished with a medium-speed microcomputer performing the FFT/PDI functions through the μFFT module on the μBus.

For missile flight tests, the warhead section and associated microcomputer is replaced by a telemetry package and similar dedicated microcomputer. The telemetry computer and its associated RTU operate as a bus monitor for digital data gathering, with the additional analog test data being input via an analog multiplexer/A-D converter (ADAC) I/O module.

Both the launch aircraft and test equipment have direct access to each microcomputer via the common bus, (e.g. MIL-STD-1553A), enabling fault isolation to the major subassembly level.

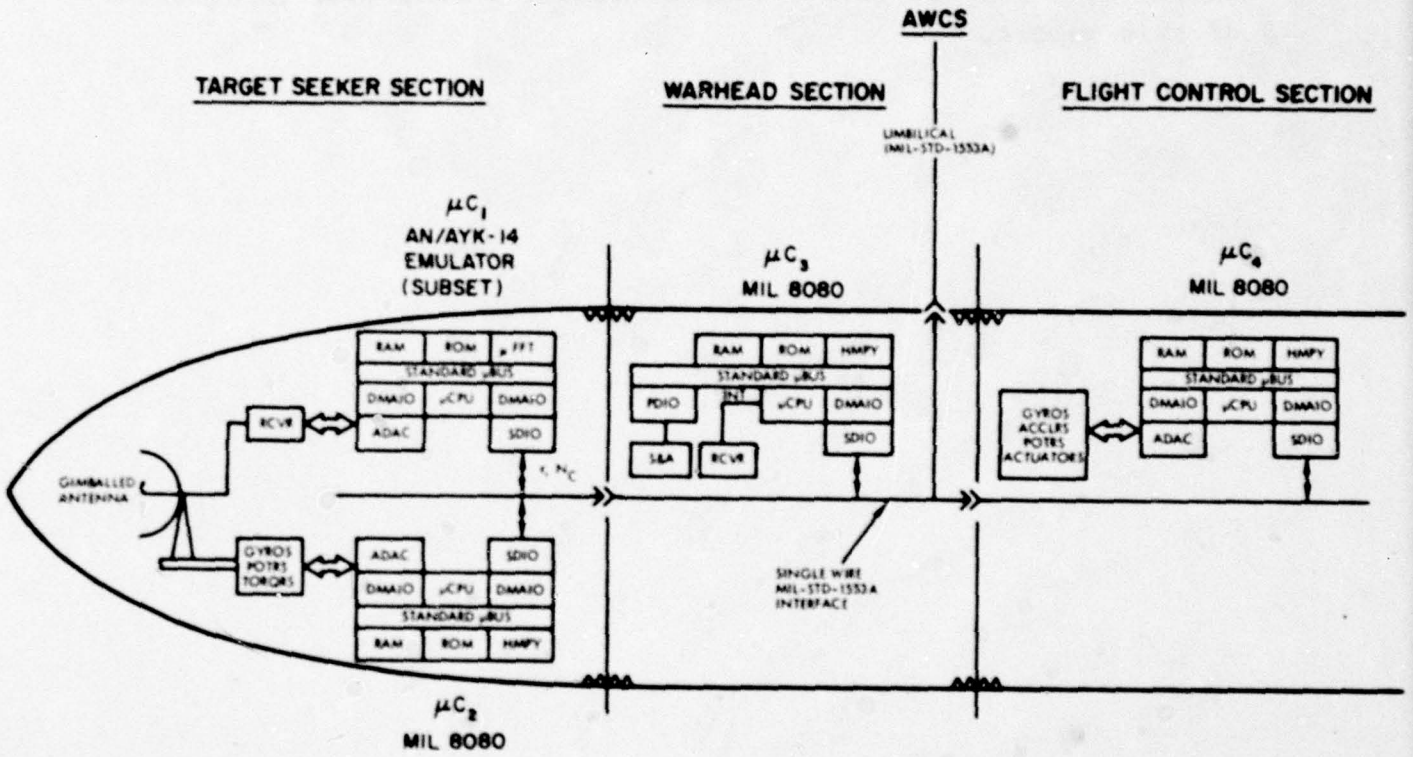


Figure 3.13 - Modular Digital Missile System

3.5 Microcomputer Macromodule Specifications

As a follow-on effort to the above described evolution of the microcomputer macromodules, alternative device technologies were explored. The results of the latter work is reflected in the critical item product function specifications contained in Section 8 of this report.

4. 8 AND 16-BIT MICROCOMPUTER SOFTWARE COMMONALITY

During the previous study phases the need was shown for a family of microprocessors to cover the range of throughput requirements in modular digital missile guidance and control. For hardware economy, particularly in federated computer systems, the low-cost, 8-bit, CPU-on-a-chip microprocessor provided an efficient watch of available throughput to low-performance missile seeker head control, fuzing and telemetry functions. However, since steering command generation involving state estimation and guidance law configurations required a higher throughput 16-bit processing capability, the question of support software compatibility was raised. This task of the study addresses the problem of common design support by investigating compatibility features in the following categories:

1. Object code
2. Source code
3. Hardware and software development aids

Give object code compatibility, the problem goes away. Compatibility at the source code level, however, implies either a common assembly language or high-order-language, with the burden placed upon a suitable translator or code generator.

4.1 Object Code Compatibility

Object code compatibility implies the ability of both 8 and 16-bit microprocessors to execute programs written in the machine code of either machine and hence demands a high degree of architectural commonality between processors.

4.1.1 Direct Compatibility

In its simplest form, such compatibility would require identical instruction sets or at least the embodiment of the 8-bit microprocessors set within the 16-bit machine's repertoire i.e. upward compatibility. Figure 4.1 illustrates this situation, which essentially means a different packing arrangement of the 8-bit fields of the instruction.

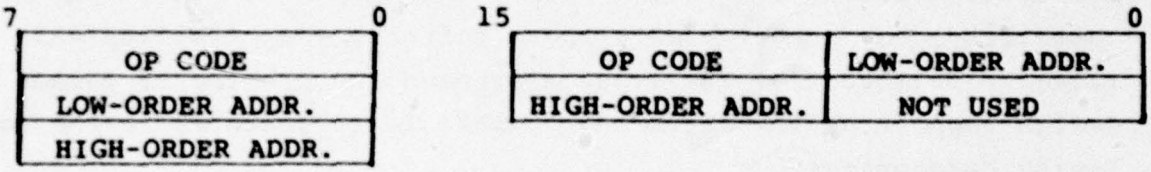


Figure 4.1 - 8 and 16-Bit Instruction Formats

4.1.2 Code Translation

The alternate to using exactly the same machine code for each machine is to interface a translator between either the output of the assembler and the main store of the microcomputer or between the main store and the control section of the CPU. The first alternative, Figure 4.2, constitutes a software approach, whereas the second is a hardware method using microprogramming techniques (Figure 4.3). Both of these alternatives are considerably more costly than direct compatibility and, as in the latter case, require that the architectural features are available in the μP to support the translated instructions.

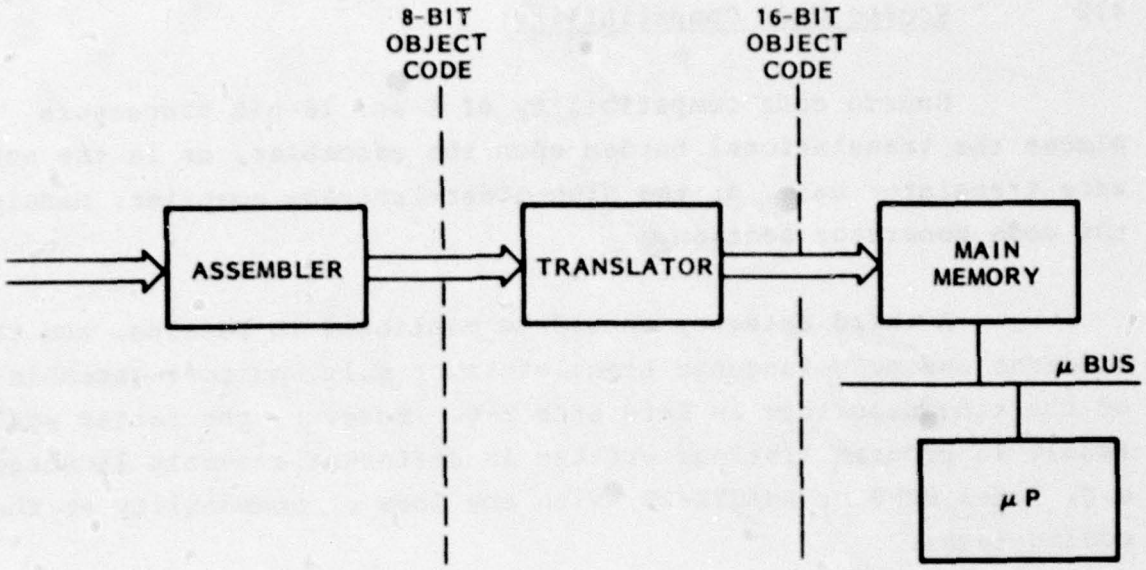


Figure 4.2 - Software Translation of Object Code

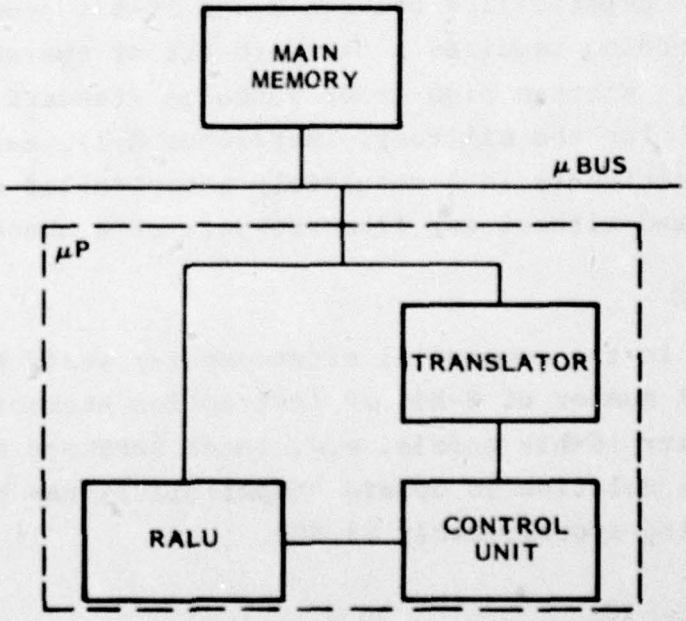


Figure 4.3 - Hardware Translation of Object Code

4.2 Source Code Compatibility

Source code compatibility of 8 and 16-bit processors places the translational burden upon the assembler, as in the software translator case, or the high-order-language compiler, namely the code generator section.

A third category should be mentioned in passing, and that concerns assembly language translators or multi-purpose assemblers of the kind described in Reference R-6. However, the latter would result in program listings written in different assembly languages, e.g. Intel 8080 or AN/UYK-20, with the loss of commonality at the coding level.

4.2.1 Assemblers

Compatibility between 8 and 16-bit processors at this level of coding requires a standard set of operation code mnemonics. Whereas high order language standardization is a distinct goal for the military, (Reference R-7), assembly language standardization is in a completely uncontrolled state at the present time and without any firm prospect of a change in the near future.

In the commercial microcomputer world there is evidence of a small number of 8-bit μP instruction mnemonics being adopted in the later 16-bit models, e.g. Intel 8080 and 8086, Table 4.1. Again, the solution to upward compatibility has been via translators costing approximately $3,500.

TABLE 4.1

8080 TO 8086 INSTRUCTION MNEMONIC COMPARISONS

8080	8086	8080	8086
STAX B	MOV DI,CX	ANI data	AND AL,data
	STOB [DI]	XRI data	XOR AL,data
LDAX B	MOV SI,CX	ORI data	OR AL,data
	LODB [SI]	CPI data	CMP AL,data
STAX D	MOV DI,DX	RLC	ROL AL
	STOB [DI]	RRC	ROR AL
LDAX D	MOV SI,DX	RAL	RCL AL
	LODB [SI]	RAR	RCR AL
SHLD addr	MOV addr,BX	DAA	DAA
LHLD addr	MOV BX,addr	CMA	NOT AL
STA addr	MOV addr,AL	STC	STC
LDA addr	MOV AL,addr	CMC	CMC
INR reg	INC reg (See Figure 2-7)	JMP addr	JMP addr*
DCR reg	DEC reg	CALL addr	CALL addr
MVI reg,data	MOV reg,data	RET	RET
MVI M,data	MOV [BX],data	RST n	CALL 8*n
MOV reg,reg	MOV reg,reg	JNZ addr	JNZ addr**
MOV M,A	MOV [BX],AL	JZ addr	JZ addr
MOV A,M	MOV AL,[BX]	JNC addr	JNB addr
LXI reg,data	MOV reg,data	JC addr	JB addr
DAD reg	LAHF	JPE addr	JPE addr
	ADD BX,reg	JPO addr	JPO addr
	RCR SI	JP addr	JNS addr
	SAHF	JM addr	JS addr
	RCL SI	CNZ addr	JZ next-inst
	or ADD BX,reg (unlike DAD—will affect AF, PF, SF and ZF)		CALL addr
		CZ addr	JNZ next-inst
INX reg	LAHF		CALL addr
	INC reg	CNC addr	JB next-inst
	SAHF		CALL addr
	or INC reg (unlike INX—will affect AF, PF, SF, and ZF)	CC addr	JNB next-inst
			CALL addr
DCX reg	LAHF	CPE addr	JPO next-inst
	DEC reg		CALL addr
	SAHF	CPO addr	JPE next-inst
	or DEC reg (unlike DCX—will affect AF, PF, SF, and ZF)		CALL addr
		CP addr	JS next-inst
POP reg	POP reg		CALL addr
PUSH reg	PUSH reg	CM addr	JNS next-inst
POP PSW	POP AX		CALL addr
	SAHF	RNZ	JZ next-inst
PUSH PSW	LAHF		RET
	PUSH AX	RZ	JNZ next-inst
PCHL	JMP BX		RET
SPHL	MOV SP,BX	RNC	JB next-inst
XTHL	POP SI		RET
	XCHG BX,SI	RC	JNB next-inst
	PUSH SI		RET
XCHG	XCHG DX, BX	RPE	JPO next-inst
ADD reg	ADD AL,reg		RET
ADC reg	ADC AL,reg	RPO	JPE next-inst
SUB reg	SUB AL,reg		RET
SBB reg	SBB AL, reg	RP	JS next-inst
ANA reg	AND AL,reg		RET
XRA reg	XOR AL,reg	RM	JNS next-inst
ORA reg	OR AL,reg		RET
CMP reg	CMP AL,reg	OUT port	OUT port
ADI data	ADD AL,data	IN port	IN port
ACI data	ADC AL,data	DI	CLI
SUI data	SUB AL,data	EI	STI
SBI data	SBB AL,data	NOP	XCHG AX,AX
		HLT	HLT

*Address on 8086 jumps and calls must be adjusted to be self-relative.

**Conditional jumps to a location out of the short self-relative range must be implemented by using a reversed-sense conditional jump around a normal jump to the location.

e.g. JNZ addr becomes JZnext-inst JMP addr

4.2.2 High-Order Language Compatibility

To date only two high-order-languages have been used for 8-bit microprocessors viz: FORTRAN IV and a subset of PL/I i.e. PLM (Intel 8080) and PL/M-6800 (Motorola M6800). Both languages are sensitive to the machine's word or byte length for arithmetic precision and hence re-targeting of the code converter for longer word length machines involves compensation for the precision required. Neither of the latter languages can be termed a "real-time" language and efficiencies can vary from 50% to 75%. Ideally, a military standard HOL such as the up and coming DOD-1 would be the preferred language for both 8 and 16-bit microprocessors.

4.3 Hardware and Software Development Aids

The 8-bit microprocessor could typically be a MIL-qualified Intel 8080, and the 16-bit machine an LSI version of the Navy AN/UYK-20 standard minicomputer using AMD 290D-Series 4-bit-slice microprocessor building blocks, or alternatively the Navy AN/UYK-30 microprocessor using the Intel 3000-Series 2-bit-slice family. While machine instruction sets could be expected to differ widely in the above cases, the question of design support in terms of a universal microcomputer development system for both 8-bit and 16-bit microcomputer system/subsystem design, development, integration and test, poses several potential commonality features, namely:

1. Multi-assembler capability
   - o Macrocode
   - o Microcode

2. Multi-high-order-language (HOL) compiler capability
   - o FORTRAN
   - o CMS-2
   - o JOVIAL J3 & J73

3. Common operating system
   - o Software development aids
   - o Hardware development aids

4. 8 and 16-Bit microprocessor remoting capability
   - o Any 8/16-bit microprocessor by replaceable module (printed-circuit board)
   - o Umbilical to tactical μC subsystem

4.3.1 Multi-Assembler Capability

In view of the significant decrease in computer hardware cost, including peripherals, the economies of time sharing cross-assemblers resident in large-scale computers versus the personal, stand-alone, microprocessor-based counterparts tilts in favor of the latter. In turn, the selection of any of the several candidate MDSs currently on the market becomes weighted in favor of systems which support a range of microprocessor types by providing the respective assemblers, either resident or hosted.

Further, since the trend is to emulate existing micro and minicomputers to meet high speed microcomputer applications, viz-a-viz the Signetics 3000 and AMD 2900 8080 emulators, and the potential missile-boone LSI AN/UYK-20 (LSI-20) microcomputer, to capture the support software, the need arises for a microcode assembler capability in the MDS. Such a microcode assembler would also be required for ongoing high-speed microprogrammed I/O controller

developments, (e.g. DMAIO, ADAC and SDIO modules), using bit-slice bipolar or CMOS-SOS microprocessor circuits. Examples of existing commerical microcode assemblers are: AMDASM and RAYASM (References R-8 and R-9), which support the AMD 2900-Series microprocessor circuit family.

4.3.2 Multi HOL Compiler Capability

At this level of programming language a greater degree of microprocessor independence is achieved in terms of software sensitivity to the type of target machine, whether an 8 or 16-bit processor. FORTRAN cross-compilers exist for several popular single-chip microprocessors, both 8 and 16-bit, (e.g. Intel 8080 and TI 9900), also the Navy AN/UYK-20 16-bit minicomputer.

The MDS is therefore a logical place to offer a choice of HOL cross compilers, as these become available for the new microcomputers. However, HOL compilers have traditionally been hosted on large/maxi computers, but with the advent of microcomputer development systems as a comprehensive development tool, it is to be expected that HOL compilers for microcomputers will eventually be hosted on next generation MDSs.

4.3.3 Common Operating System

Microcomputer system development can be divided into at least three distinct phases (see Figure 4.4):

- Software design and debug
- Hardware design and debug
- Hardware and software integration and test

Development aids should assist the efforts in all phases.

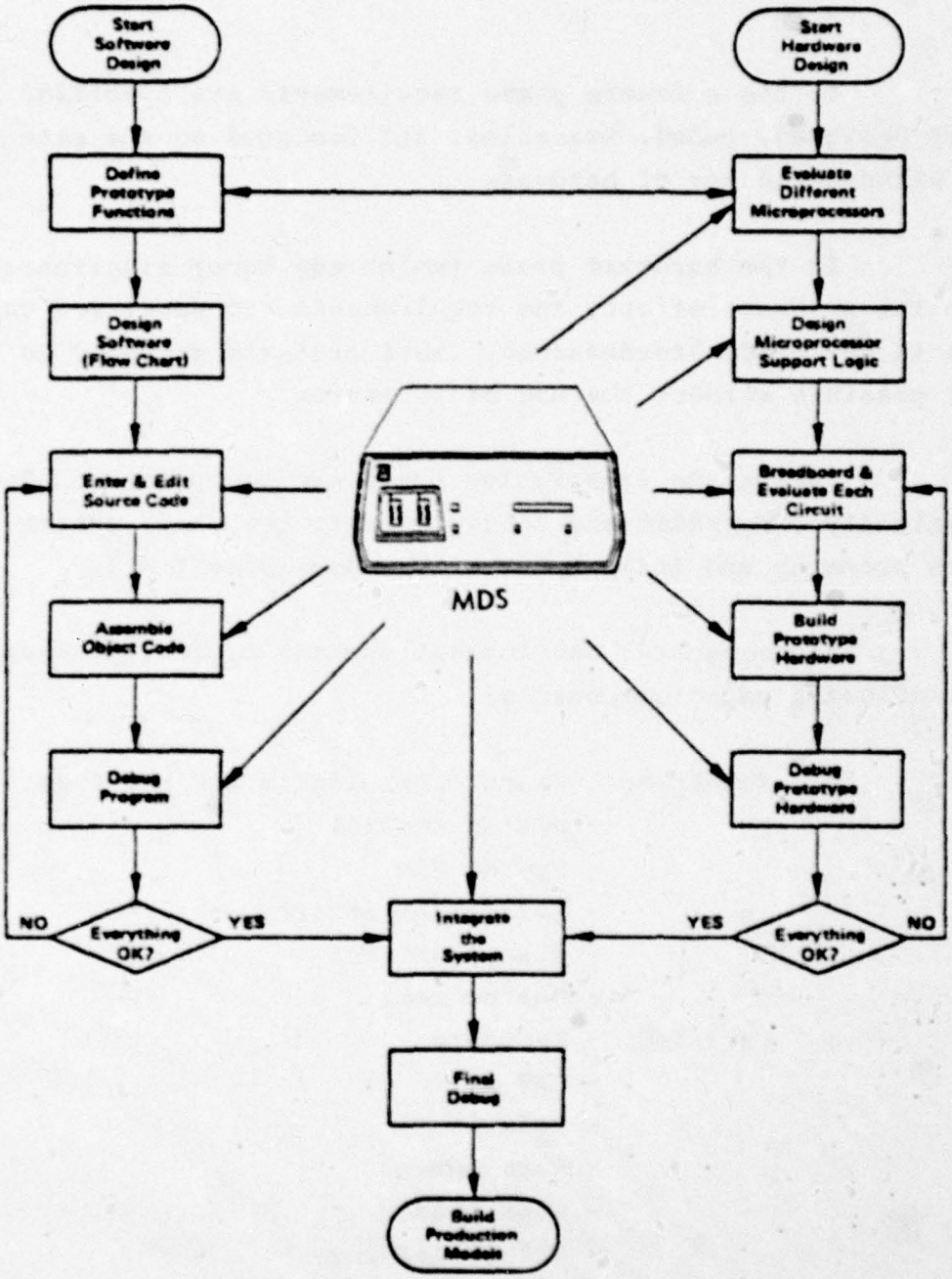


Figure 4.4 - µComputer Development Cycle

In the software phase requirements are specified and programs designed, coded, assembled, and debugged to the extent possible without the use of hardware.

In the hardware phase (which may occur simultaneously with the software effort) the requirements are specified and hardware is designed, breadboarded, fabricated and debugged to the extent possible without the use of software.

During the integration phase microcomputer modules are systematically integrated and debugged until the whole system functions properly and independent of the development aid.

Microcomputer development systems typically consist of the following major components:

- o Mainframe
  - Front panel lights and switches
  - System control
  - System RAM
  - Peripheral interfaces
  - Trace hardware
  - Bus control
- o User I/O
  - Keyboard
  - CRT
  - Printer
  - Tape punch
  - Tape reader
  - TTY (Teletype)
  - Mass storage (diskett or cassette)
- o Software
  - Editor
  - Assembler
  - Compiler

- Linker
- Debugger
- Disassembler
- Operating System
- File Manipulation
- User Programs

o Hardware Interface
- Emulator Processor
- Emulator Clock
- Emulator I/O
- Emulator RAM, PROM, ROM
- PROM Programmer
- Hardware Probes
- Interface Cable

The mainframe is the system's central node to which all other subsystems are attached and through which other subsystems are controlled. It generally consists of a rack mountable box into which various standard and optional circuit cards may be plugged.

User I/O provides the articulatory channels through which the system under development can be internally manipulated and observed.

The operating system is the software's interface between the engineer/programmer, hardware and the functional software components. It performs peripheral control functions and commands the use of the editor, assembler, linker, etc..

Software development (user program design, coding and debug) requires the use of the editor (source file creation and modification), assembler (Assembly Language to Machine Language

converter), compiler (HLL to Machine Language converter), linker (concatenates Machine Language code segments), File Manipulator (maintains disc or tape file library), debugger (permits real-time breakpoint, trace, trap, probe interrupt, execution control and program modification) and disassembler (reconverts machine language code-such as generated by a trace-back to assembly language syntax).

4.3.4 8 and 16-Bit Microprocessor Remoting Capability

The hardware interface is the umbilical link between the development aid and the system under development. Typically the CPU is removed and the interface cable plugs into the CPU's socket. Initially, debugging commences while RAM, PROM, ROM, clock, and I/O ports are removed from the system under development. Using test software or the final system software, located along with RAM, PROM, ROM, clock and I/O surrogates in the mainframe, the hardware is checked out and debugged. One by one the clock, I/O and RAM are inserted into the system and made to work properly. Next the debugged program is placed into PROM or ROM. Finally the development aid's hardware interface is removed from the CPU socket and replaced by the CPU itself the development process is complete.

An examination of Table 4.2 indicates that development aids are available for almost all microcomputers (μCs). They are a necessary marketing tool without which users would find μC use difficult to impossible.

Table 4.2 shows the commonality capabilities of two "universal" development aids for 2, 4, 8 and 16-bit μC's.

TABLE 4.2

μC DEVELOPMENT AID COMMONALITY

Device	Mfg.	Intel MDS		Tektronix 8002		# Bits
		Software	ICE	Software	ICE	
3000	Intel	X	X			2
2901	AMD	X				4
8080	Intel	X	X	X	X	8
8085	Intel	X	X			8
Z80	Zilog	R	R	X	X	8
8048	Intel	X	X			8
8748	Intel	X	X			8
8035	Intel	X	X			8
6800	Motorola	(R)	(R)	X	X	8
68000	Motorola					16
8086	Intel	(X)	(X)			16
Z8000	Zilog					16
9900	TI	(R)	(R)	X	X	16
μNOVA	DG					16
LSI-11	DEC					16
High-Speed Emulators:						
8080	Signetics	X		X		8
9080	AMD	X		X		8
AN/AYK-14	CDC					16
AN/UYK-30	Hughes		X			16

Key: ICE = in-circuit emulator
X = available
R = available via RELMS
() = to be announced

Unfortunately μC development tools are fairly costly - to the extent that μC selection is greatly influenced by the user's cost of access to a compatible development aid.

Microcomputer manufacturers furnish development systems which are exclusively compatible with their own microprocessors. In this way a customer purchases a single development tool which can service a product line of μC types.

One major electronic laboratory instrument manufacturer, (Reference R-10), has produced a "universal" development aid, with the potential of being compatible with all popular μC's. Certain other manufacturers, (Reference R-11), offer plug-in modification cards which enable the use of the Intel MDS development aid with other μCs.

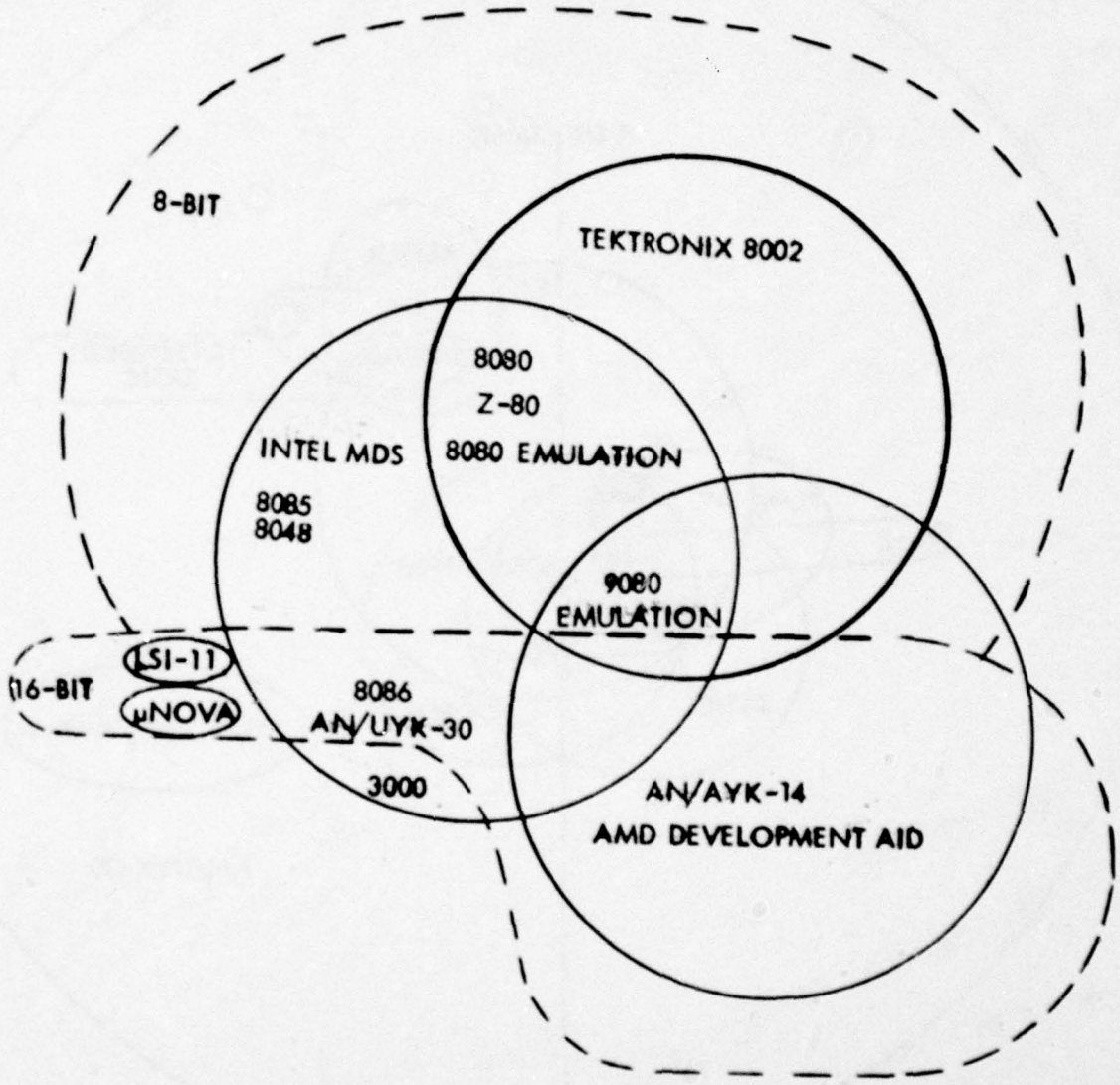


Figure 4.5 - Venn Diagram - Development Aid Commonality

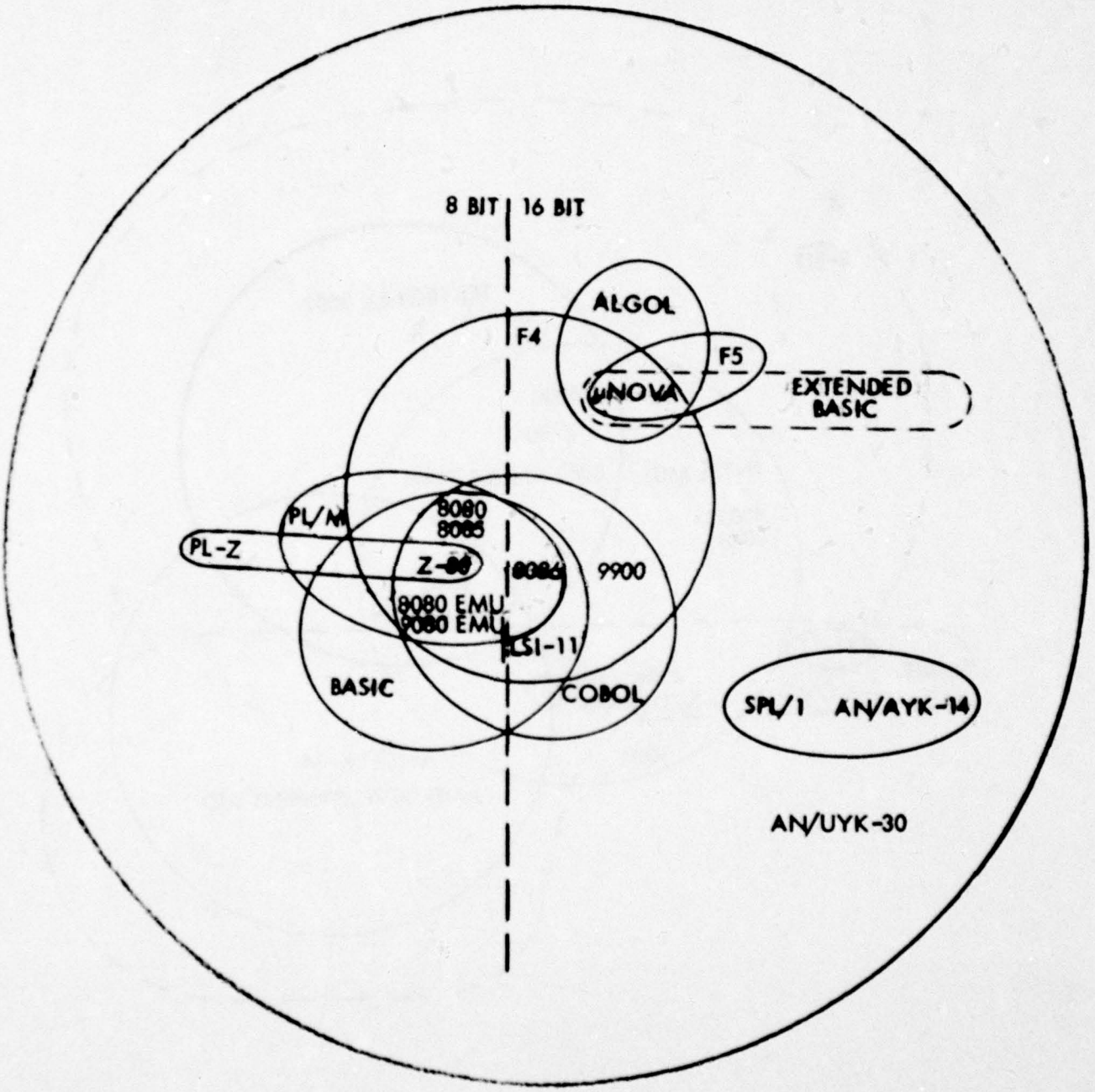


Figure 4.6 - Venn Diagram - Higher Level Language Commonality

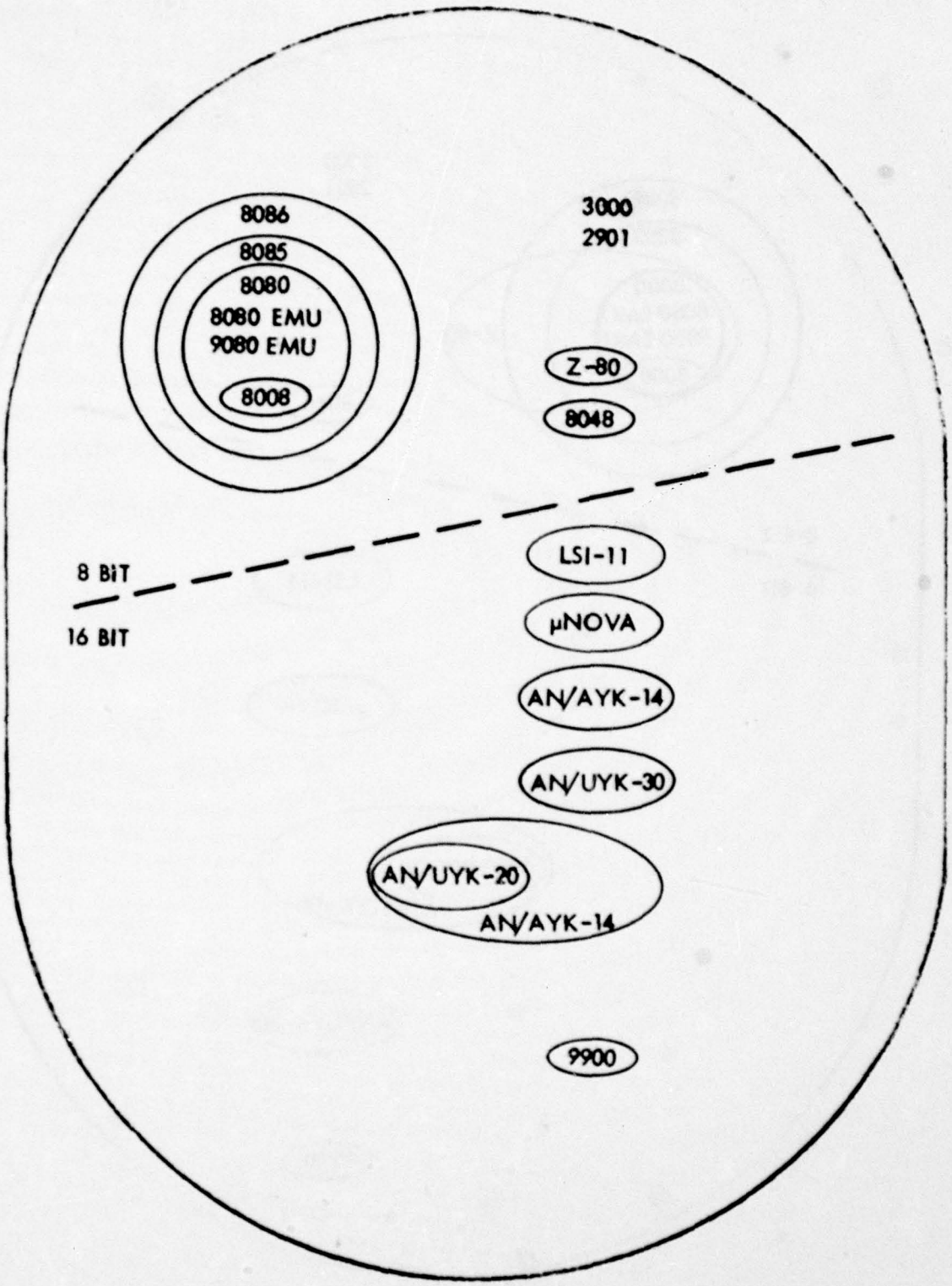


Figure 4.7 - Venn Diagram - Assembly Language Instruction Set Commonality

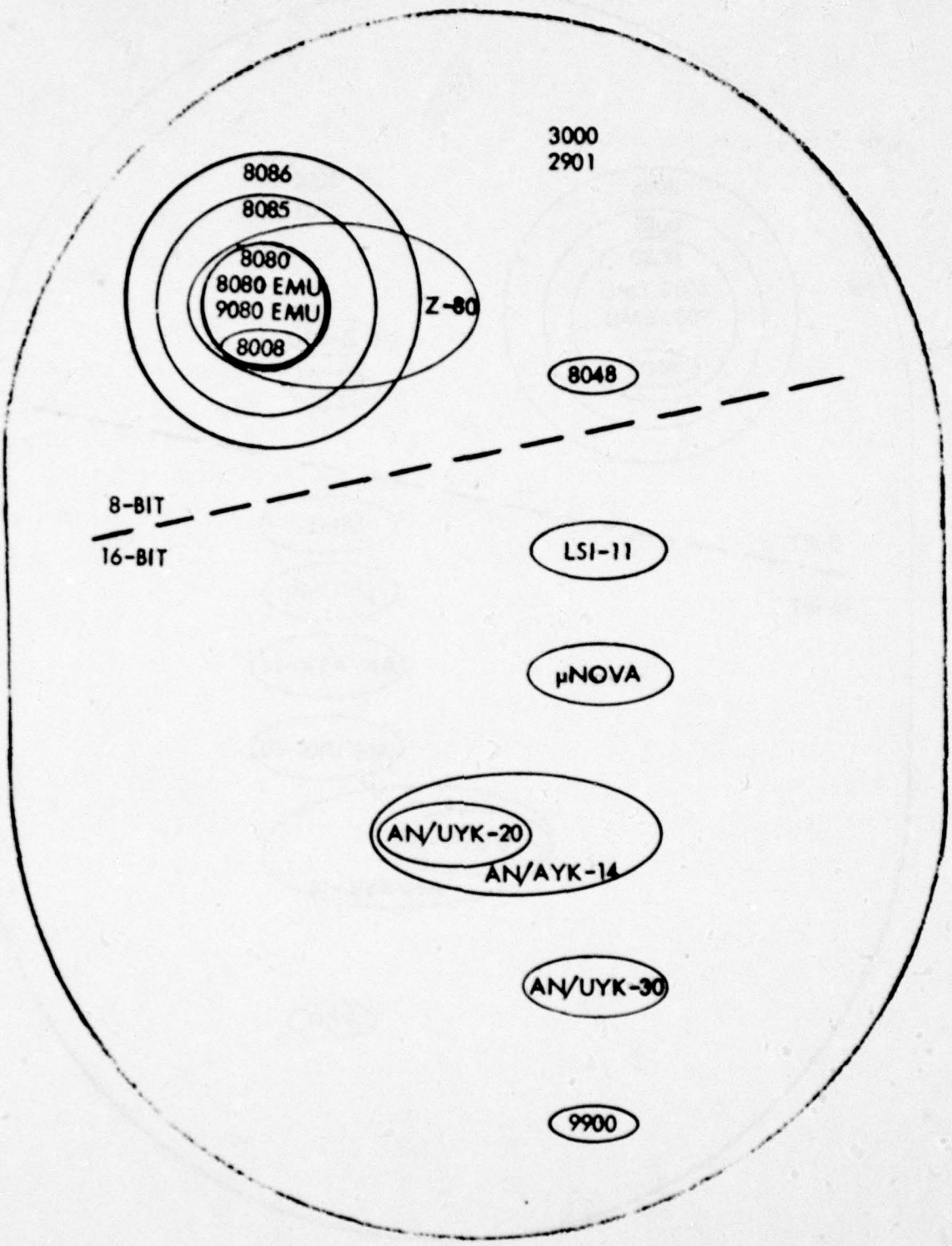


Figure 4.8 - Venn Diagram - Machine Language Instruction Set Commonality

5. AN/UYK-30 PERFORMANCE AND COMMONALITY

Since no small (LSI) avionics of the Navy 16-bit AN/UYK-20 and AN/AYK-14 minicomputers currently exists for missile applications, the Navy AN/UYK-30 bit-slice, microprocessor was evaluated as a potential candidate for the high-speed microprocessor (μP) module in the macromodular microcomputer family. The AN/UYK-30 microprocessor was designed and developed under a NAVAIR contract (Ref. R-12) to provide a digital autopilot for the Phoenix missile.

5.1 AN/UYK-30 Major Characteristics

The central processing unit (CPU), is packaged on six SEM-2A modules (Figure 5.1) in addition to other packaging configurations.

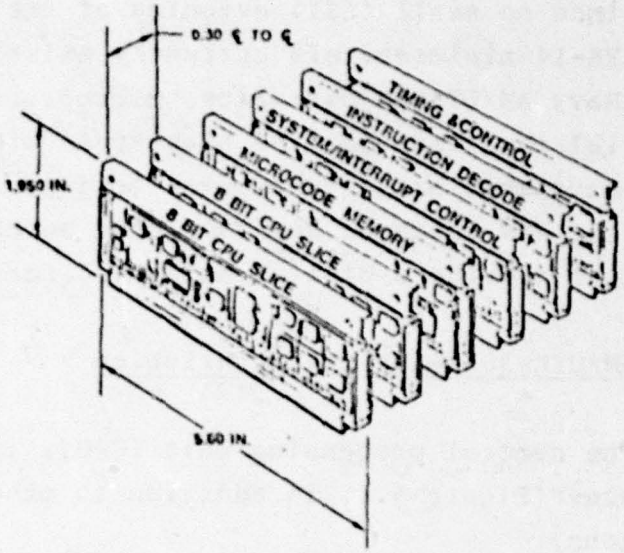


Figure 5-1 AN/UYK-30 SEM-2A Packaging

A performance profile of the AN/UYK-30 is given in Table 5.1 and its basic architecture is shown in Figure 5.2.

TABLE 5.1
AN/UYK-30 MICROPROCESSOR CHARACTERISTICS

Parameter	Specification
Number System	Binary, Fixed-point
Arithmetic Mode	2's complement fractional
Wordlength	16-bits
Operating temperature range	Mil spec (-55° to +125°C)
Approximate throughput	300 - 600 KOPS
Technology	Low-power Schottky bipolar (T^2L)
System clock	4 MHz (50 nsec pulse width)
Power supply voltage	+5 vdc
Logic levels	T^2L voltages
Power consumption	16W (typ)/24 W (max)
IC count	70
Card count (brassboard)	3 (6.5" x 5.5" x 0.5" cards)
(productized PCB)	2 (5.65" x 6.3" x 0.4" cards)
(productized SEM 2A)	6 (5.6" x 1.95" x 0.3" cards)

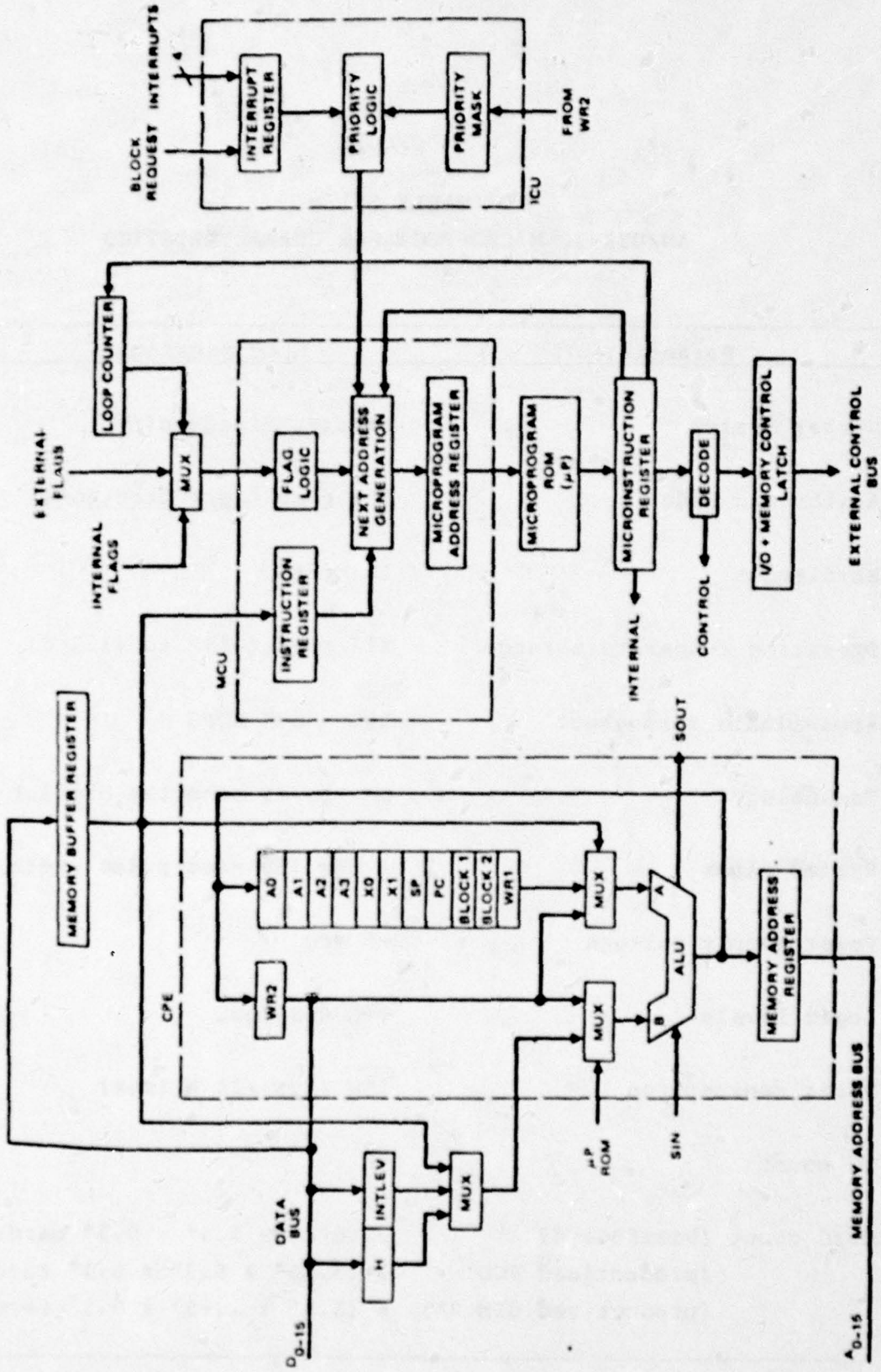


Figure 5.2 - AN/UYK-30 Microprocessor Block Diagram

5.1.1 CPU Registers

The AN/UYK-30 central processing unit (CPU) has very few registers available for general use. Since the PC and SP registers are dedicated, only six registers are "available". However, two are used for indexing which is somewhat of a drawback, and the other four are assigned to arithmetic calculations. By comparison, the PDP-11/34 has six registers available but all are multi-purpose and all can be used for indexing.

5.1.2 Instruction Set

The AN/UYK-30 instruction set (Table 5.2) is adequate for missile guidance computations however, a few points are worth noting. Certain "convenience" instructions are available, such as a double-precision ADD, while some others were missing, such as an Increment Register and/or Increment Memory instruction.

Curiously, the shift register instructions are slow. In most machines a "shift left nineplaces" instruction is significantly faster than multiplying by 512. On the AN/UYK-30, a shift of nine or greater places can take longer than the corresponding multiplication.

TABLE 5.2

AN/UYK-30 INSTRUCTION SET

INSTRUCTION	INSTRUCTION TIME (μsec)		ADDRESSING MODES
	FAST MEMORY*	SLOW MEMORY**	
MEMORY REFERENCE			
ADD	1.5	2.25	DIRECT, INDEXED
ADD DOUBLE	2.25	2.75	DIRECT, INDEXED
AND	1.75	2.25	DIRECT, INDEXED
COMPARE	2.0	2.5	DIRECT, INDEXED
DIVIDE	20.25	20.5	DIRECT, INDEXED
LIMIT	3.5	4.0	RELATIVE
LOAD	1.5	2.25	DIRECT, INDEXED, REL., REL. INDIR.
MULTIPLY	10.5	10.75	DIRECT, INDEXED
OR	1.75	2.25	DIRECT, INDEXED
STORE	2.0	3.5	DIRECT, INDEXED, REL. INDIRECT
SUBTRACT	1.5	2.25	DIRECT, INDEXED
REGISTER - REGISTER			
ABSOLUTE VALUE	2.5	3.0	REGISTER
ADD REGISTER	1.5	2.0	REGISTER
AND REGISTER	1.75	2.0	REGISTER
COMPARE REGISTER	2.0	2.5	REGISTER
COMPLEMENT	2.0	2.0	REGISTER
MOVE	1.5	2.0	REGISTER
NEGATE	2.0	2.5	REGISTER
OR REGISTER	2.0	2.0	REGISTER
POP STACK	2.75	3.25	STACK
PUSH STACK	2.5	3.5	STACK
SUBTRACT REGISTER	1.5	2.0	REGISTER
SHIFT			
ROTATE	2.75 + .75N***	3.25 + .75N***	IMMEDIATE
SHIFT LEFT	2.5 + .5N	2.5 + .5N	IMMEDIATE
SHIFT LEFT DOUBLE	3.25 + N	3.25 + N	IMMEDIATE
SHIFT RIGHT	2.5 + .5N	2.5 + .5N	IMMEDIATE
SHIFT RIGHT ARITH.	2.75 + .5N	3.25 + .5N	IMMEDIATE
SHIFT RIGHT DOUBLE	4.25 + .75N	4.25 + .75N	IMMEDIATE
BRANCH			
BRANCH NEGATIVE	2.0	2.5	RELATIVE, REL. INDIRECT
BRANCH NOT ZERO	2.0	2.5	RELATIVE, REL. INDIRECT
BRANCH POSITIVE	2.0	2.5	RELATIVE, REL. INDIRECT
BRANCH ZERO	2.0	2.5	RELATIVE, REL. INDIRECT
INCREMENT & BRANCH IF ≠ 0	2.25	2.75	RELATIVE
JUMP	1.75	2.25	RELATIVE, REL. INDIRECT
JUMP SUBROUTINE	2.0	3.0	RELATIVE, INDIRECT, REL. INDIR.
SKIP IF "AND" ZERO	2.75	3.75	DIRECT, INDEXED
IMMEDIATE			
ADD IMMEDIATE	1.25	1.75	IMMEDIATE
COMPARE IMMEDIATE	2.0	2.5	IMMEDIATE
LOAD IMMEDIATE	1.25	1.75	IMMEDIATE
INPUT/OUTPUT			
INITIATE BLOCK TRANSFER	2.5	3.25	DIRECT
PARALLEL IN	2.25	2.5	INPUT/OUTPUT
PARALLEL OUT	2.25	2.5	INPUT/OUTPUT
PULSE OUT	2.25	2.75	INPUT/OUTPUT
SERIAL IN	6.5	7.0	INPUT/OUTPUT
SERIAL OUT	6.5	7.0	INPUT/OUTPUT
SKIP IF I/O READY	2.75	3.25	INPUT/OUTPUT
CONTROL			
INTERRUPT MASK	1.75	2.0	IMMEDIATE
LOCK	2.75	3.75	DIRECT
RETURN INTERRUPT	3.5	5.25	IMPLIED
RETURN SUBROUTINE	2.75	3.75	IMPLIED

*MEMORY ACCESS LESS THAN 160 NSEC

**MEMORY ACCESS LESS THAN 560 NSEC

***N = NUMBER OF PLACES SHIFTED MINUS ONE

5.2 AN/UYK-30 Evaluation

The evaluation of the AN/UYK-30 as a suitable candidate for the high-speed μP module was performed in accordance with the following sub-tasks:

1. Benchmark program performance.

2. Electrical interface with ONR microbus (μBus) and associated macromodules.

3. Packaging compatibility with ONR macromodules.

5.2.1 Benchmark Program Performance

As in the Phase III study for the AN/UYK-20 and PDP-11/34 computers, the Angle Track Error program module (SP-16) was used as the benchmark program to assess the AN/UYK-30 performance for missile steering command generation (SCG). Support software for coding the program on the AN/UYK-30 was limited to a symbolic assembler.

The AN/UYK-30 assembler, resident on a floppy-disc, was obtained from the Naval Avionics Facility, Indiannapolis (NAFI), together with supporting documentation (Ref. R-13). An in-house Intel Microprocessor Development System (MDS) was used to generate AN/UYK-30 object code from the benchmark program written in AN/UYK-30 assembly language.

By comparison the PDP-11/34 has one clear advantage with its assembly language, namely the "PC addressing mode" which creates multiword instructions with indirect addresses provided by the assembler. On the AN/UYK-30, the programmer must create indirect words as constants and keep track of them when coding. For compiler use, naturally this feature is transparent to the programmer, and loses its advantage.

The benchmark was coded twice: once using software floating-point arithmetic and again using fixed-point calculations.

Software Floating-Point Arithmetic - To perform floating-point calculations on the AN/UYK-30, a number of software floating-point routines were written. Formats were designed to be identical to PDP-11/34 floating-point arithmetic with subroutine calls substituted for the non-existent floating-point instructions. A comparison of execution times is shown in Table 5.3. In addition to being more than ten times slower, the lack of special floating point registers required extra instructions to load normal registers for inputs to the floating-point subroutines. The penalty is approximately fifty percent more storage required for AN/UYK-30 floating point calculations.

TABLE 5.3

COMPARISON OF *EXECUTION TIMES OF AN/UYK-30, PDP-11/34 AND AN/UYK-20.

Processor		Execution Time (μsec)
AN/UYK-30	(160 ns. memory cycle)	2250
	(660 ns. memory clcle)	2956
PDP-11/34	(assembler)	379
AN/UYK-20	(assembler)	460

NOTES:

* Execution time of program SP14, using a "typical pass" in which there was no jamming, and target detection in one Doppler Cell.

TABLE 5.4

FLOATING-POINT COMPARISON OF AN/UYK-30 VS. PDP-11/34.

EXECUTION TIMES (μsec)

Floating-Point Instruction	AN/UYK-30 Software		PDP-11/34 Hardware
Memory:	160 nsec	660 nsec	
Load and Convert Integer to Floating-Point	79.25	103	5.53
Addition	152.75	209	9.87
Multiply	135.5	182.25	7.87
Divide	171.75	212.25	13.7

Fixed-Point Arithmetic - The results shown in the previous paragraph show the AN/UYK-30, using software floating-point calculations, to be approximately six times slower than the PDP-11/34 when executing a typical program section. To avoid unfairly penalizing the AN/UYK-30 for its lack of floating-point hardware, the "typical program section" was recoded using software fixed- point calculations and the results are listed in Attachments Tables 5.6 and 5.7. The "typical program section" execution time was roughly halved, using fixed-point making the AN/UYK-30 about three times slower than the PDP-11/34.

Fixed-point arithmetic was performed using a fixed 16-bit integer and 16-bit fraction, corresponding to the 32-bit precision used in the floating-point calculations.

In its favor, the AN/UYK-30 has three double-precision instructions which were useful in both the fixed-point and floating-point routines viz:

a. Double precision ADD
b. Shift left double
c. Shift right duble

Table 5.5 gives the sizes of the "typical program section" when coded for PDP-11/34 and the AN/UYK-30.

TABLE 5.5

PROGRAM *SIZE OF "TYPICAL PROGRAM SECTION"

Processor	16-bit words
PDP-11/34 (assembler)	175
AN/UYK-30 (assembler with floating-point)	276
AN/UYK-30 (assembler with fixed-point)	265

NOTE

* Sizes do not include the software arithmetic routines.

TABLE 5.6

COMPARISON OF *BENCH-MARK EXECUTION TIMES OF AN/UYK-30 (FIXED-POINT AND FLOATING-POINT), PDP-11/34 AND AN/UYK-20.

Processor	Execution Time (μsecs)
AN/UYK-30 (using software fixed-point calculations)	
160 nsec memory cycle:	1145
660 nsec memory cycle:	1324
AN/UYK-30 (using software floating-point calculations)	
160 nsec memory cycle:	2250
660 nsec memory cycle:	2956
PDP-11/34 (with hardware floating-point)	379
AN/UYK-20 (with hardware floating-point)	460

NOTES

* Execution time of program SP14, using a "typical pass" in which there was no jamming, and with target detection in one Doppler Cell.

TABLE 5.7

ARITHMETIC COMPARISON OF AN/UYK-30 VS. PDP-11/34,
WITH AN/UYK-30 FIXED-POINT VS. FLOATING-POINT.

INSTRUCTION[1]	EXECUTION TIME[2] (μsecs)		
	AN/UYK-30 Floating-Point Software	AN/UYK-30 Fixed-Point Software	PDP-11/34 Hardware
Add	153(209)	2.25(2.75)[3]	9.87
Multiply	136(182)	67(79)	7.87
Divide	172(212)	114(130)	13.7

NOTES:

1) All instruction times are for 32-bit precision calculations.

2) AN/UYK-30 instruction times are given for two different memory speeds, fast 160 nsec cycle time, and slow 660 nsec cycle time. The execution times using the slower memory are given in parentheses.

3) The fixed-point 32-bit precision ADD is simply an AN/UYK-30 double-precision addition instruction, DADD.

5.2.2 Electrical Interface with μBus

The second aspect of the AN/UYK-30's suitability for adoption as a high-speed central processing unit in the macro-modular micro computer family lies in the electrical interface of the CPU with the ONR μBus. Figure 5.3 shows the AN/UYK-30 interface lines and Figure 5.4 shows the ONR μBus interface requirements. The chief difference between the two is in the line of partitioning chosen between the simple semiconductor memory interface, which has to be met in any event, and the memory - synchronizing timing and control circuits. Figure 5.5 illustrates the latter point.

The following paragraphs take into consideration both the software and hardware implications of incorporating the AN/UYK-30 CPU within the macro-modular micro computer family.

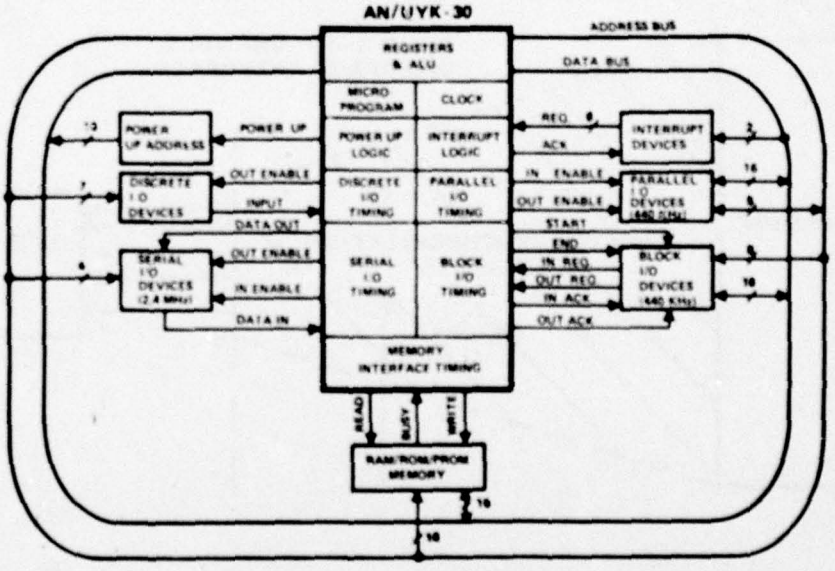


Figure 5.3 - AN/UYK-30 CPU Interface

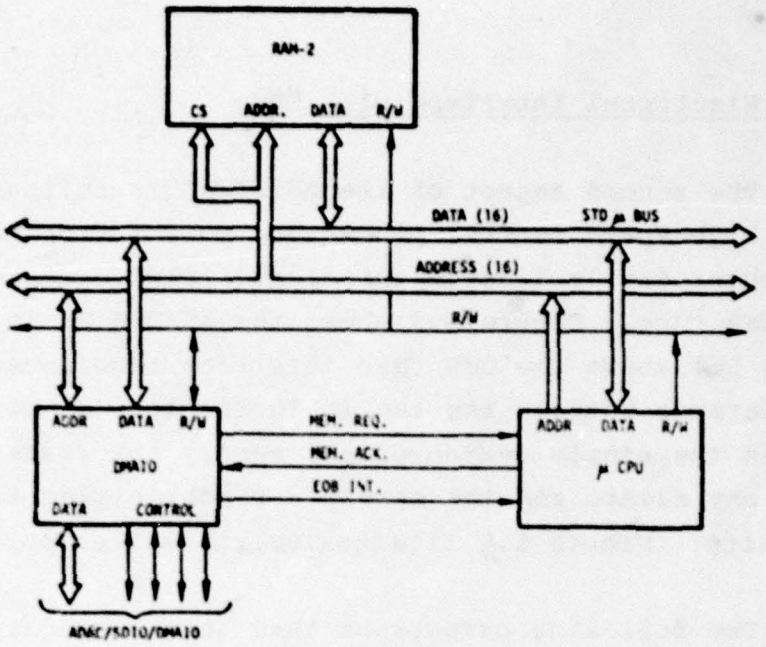


Figure 5.4 - ONR $^{\mu}$Bus Interface

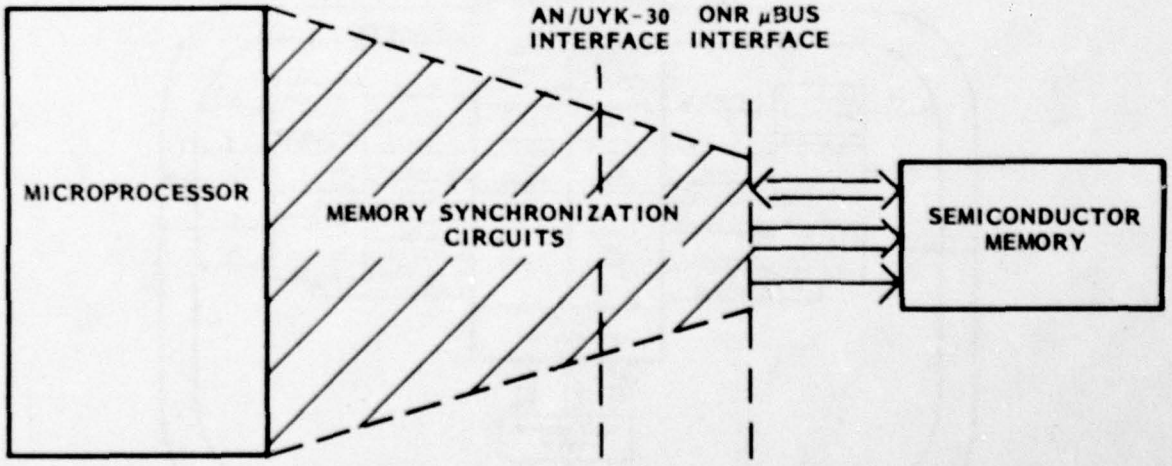


Figure 5.5 - AN/UYK-30/ONR $^{\mu}$Bus Interface/Partitioning

DMA OPERATIONS - The AN/UYK-30 contains a single channel direct memory-access (DMA) capability. The word count and address registers are contained within the unit. These registers are loaded and controlled by the BLOC instruction. The BLOC instruction specifies the location of a two-word semaphor specifying the block length and word count to be used in the transfer. Upon completion of this instruction, a Block Start pulse is sent to the external device. The external device, when ready, raises the BLOCK IN/OUT request line. After the CPU acknowledges via a BLOCK IN/OUT ACK, the CPU places the memory address on the address bus and the external device places/receives data from the data bus under control of the MEMR, MEMW signals. The difficulties here are:

- o CPU controls address lines.
- o Only one DMA channel is provided.
- o End of Data Interrupts are internal to the CPU.
- o BLOC instruction operation assumes unique dedicated DMA logic.
- o CPU maintains word count register.
- o No DMA status monitoring is provided.

In order to mate the AN/UYK-30 to the μBus, the DMA portion of the AN/UYK-30 associated with Word Count, Memory Address Register, and BLOCK IN/OUT interrupts must be deleted. The DMA initiate command BLOC must also be removed.

All of this logic is contained in the ONR DMAIO module. Two DMA channels are required for the application, and all of the normal DMA functions of load WC, MAR, etc., will be contained in these modules.

The loading, DMA starting, DMA status monitoring are then accomplished by using direct memory operations of the form STA, AAA; LDA, AAA - where AAA is the address of the DMAIO register. The DMA start command, which is normally a result of the BLOC instruction, can be generated by a direct memory write to the DMA start/stop register.

A DMA control signal multiplexer is required to translate the DMAIO module lines of MEM REQ/ACK and direction to the AN/UYK-30 lines of BLOCK IN REQ, BLOCK OUT REQ, BLOCK IN ACK, BLOCK OUT ACK. This assumes, of course, that after the deletion of the DMA logic cited above, the external controls remain unaltered. In order to ensure that the external DMAs have bus control, a DMA CYCLE signal must be generated to inhibit the AN/UYK-30 address and memory control lines. This requirement poses no difficulty for BLOCK IN requests but it does for BLOCK OUT requests. The difference here is for BLOCK IN, the external DMAIO module knows when to put the memory address on the bus via the BLOCK IN ACK. However, in the BLOCK OUT case, the ACK comes out after the fact, and the DMAIO module does not know when to place the Memory Address on the bus. (See timing diagrams, Figures 5.6 & 5.7)

Only one desirable alternative is possible. The line indicating the beginning of a BLOCK OUT cycle, or a DMA CYCLE begin, must be brought out from the AN/UYK-30. This line should go active either at or slightly before MEMR. This will allow the DMAIO module sufficient time to place the address of the desired memory cell on the bus.

Another solution would be for the DMAIO to route the address of the memory request through the AN/UYK-30. This approach is undesirable and foreign to the building block technique.

Logic on the absence of a "New Instruction" pulse after a MEMR could be done to deduce the current MEMR is scheduled for the DMA and not the CPU. This would be cumbersome and moderately complex. The most straight-forward solution is to just bring out the DMA begin cycle strobe.

Instruction Set Utilization - The instruction set peculiar to the CPU operations such as ADD, SUB, INDEX REGISTER manipulations, etc., are adaptable without modifications. Nearly all of the I/O instructions together with the interrupt handling instructions will either not be used or modified. The "not used" means the functions are to be retained; the difference in implementation is substantially different.

Input/Output instructions - All of the I/O instructions have I/O device address fields encoded in the instruction. The I/O devices typically decode this specific field to determine the action required. The Macro Module approach treats all I/O identically as memory negating the need for any special I/O fields in the instruction word. An I/O device is assigned a bank or series of address that it is responsive to. These addresses are specific memory addresses. When the programmer desires to execute a parallel input, for example, an LDA, AAA is used. Since all I/O, including memory, is on the same μBus, it appears to the programmer that the data came from memory. This approach negates the need for a special class of I/O instructions.

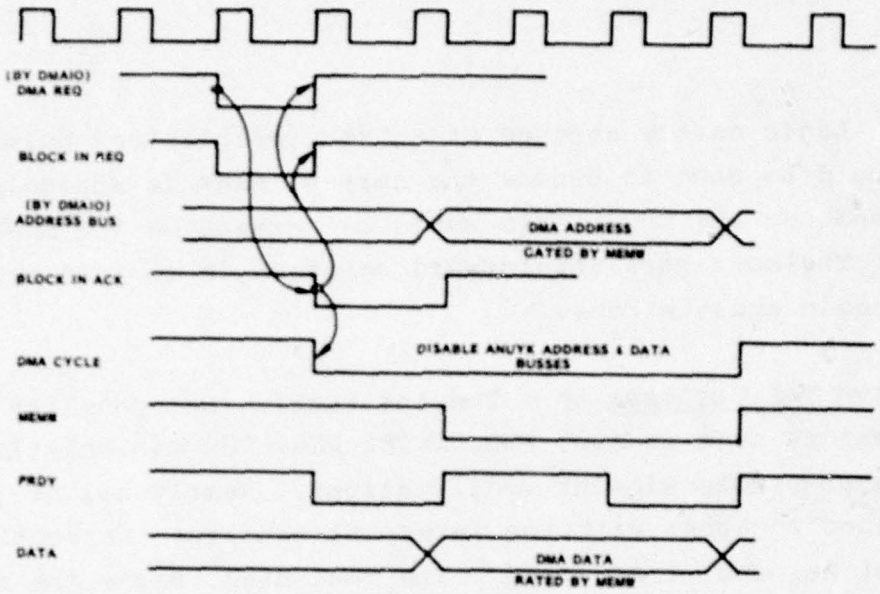


Figure 5.6 - DMA Block in Transfer Timing

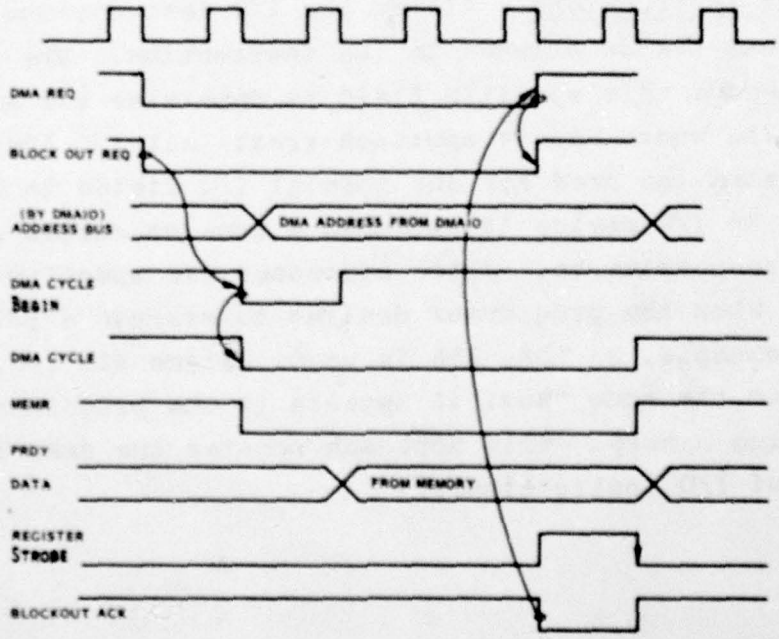


Figure 5.7 - DMA Block Out Transfer Timing

INPUT/OUTPUT INSTRUCTION DISPOSITION

Instruction	
POUT, PIN	These instructions may be conveniently replaced by direct memory writes to the appropriate PDIO module.
SIN, SOUT	The serial I/O unit, together with the SIN, SOUT instructions, are to be replaced by the SDIO module. The activation and control of the SDIO unit is controlled by direct memory reads and writes.
SKIP I/O Not Ready	This function is implemented by executing a direct memory read from the addressed device. The execution of a Branch A ≠ 0 will cause the proper skip.
BLOC	This instruction is to be deleted.

Interrupt Structure - The AN/UYK-30 provides both internal and external interrupts. The internal ones include Halt, Power Fail, BLK OUT, and BLK IN. There are four external interrupts supplied to the user. The BLK OUT/IN interrupts are generated by the internal DMA. Since external DMAIO will be used, it will be necessary to delete these interrupts from the priority tree. The rationale here is that multiple DMA units are to be implemented, and external pri-

ority logic will be used to control the various End of Data processing conditions. The DMAIO module supplies only one EOB and assumes that normal program housekeeping can determine the transfer direction.

The Interrupt mask function can be accomplished by utilizing a register in the PDIO module. The mask may be loaded by a direct memory write. This register may also be used to perform the Arm/Disarm, Enable/Disable interrupt functions. This operating mode allows for interrupt pending operations to be performed.

Since the number of interrupts exceeds the machine capacity, interrupt vectoring will be required. This may easily be done by using a PDIO module where the interrupt status can be readily determined. The AN/UYK-30 normally acknowledges an interrupt by generating the Interrupt Acknowledge signal with the current interrupt being processed encoded in data bits 14 and 15. This is adequate for non-expanded interrupts; however, the resetting of the vector needs to be done. The IOCP instruction may be used to reset each individual interrupt bit.

Memory Timing - The basic memory timing diagram is shown in Figure 5.8. The CPU places the address of the memory all on line gated with a MEMR or MEMW command. Memories and devices faster than 500 ns do not need logic on the device busy line. Since this will be the case for most memories used, no logic is necessary. For the unusual case of slow memories, the Memory Interface module will contain a counter delay register. This delay will be used to maintain a "not ready" status to the CPU for the duration of the memory cycle. The case of a slower memory used in conjunction with a fast Macro Module presents difficulties in delaying the cycle. The problem here is that although a delay for data to or from memory

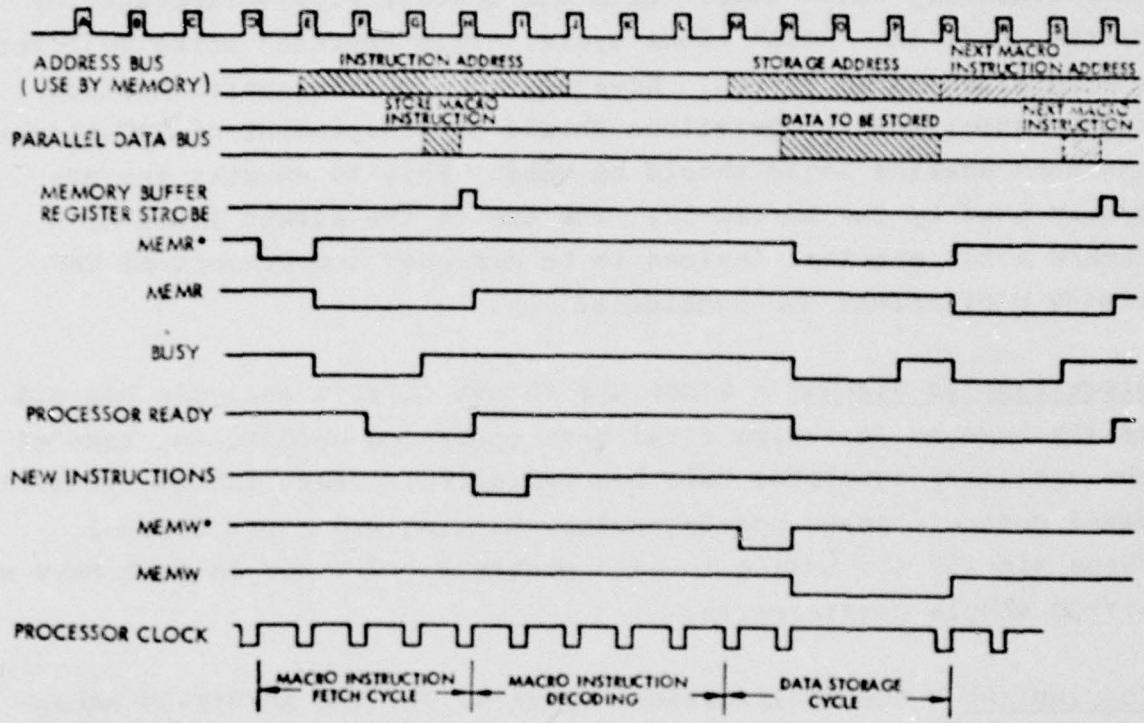


Figure 5.8 - Timing Diagram for Store Indexed Instruction

is required, data to or from the module requires no delay or a different delay. The problem is resolved by incorporating a "device not busy signal bus" in all Macro Modules.

Now, when a MEMR/W is generated to the slower memory, the memory delay counter is activated. However, when a MEMR/W is directed to a fast Macro Module, the delay is terminated by the faster device.

In the ONR μBus, the memory access lines are Address, Data, Read/Write. Generally, in a dedicated system, the data read is an open-ended read. Data is assumed valid for sampling after

some arbitrary clock time. Data and address ripples through the system until the "next" clock cycle. This approach works well for a single dedicated system. However, in a quasi general applications sense, memory operations should be independent of CPU clocks and hand shaking logic should be used. This is exactly the approach used by the AN/UYK-30. The use of the direct lines of MEMR/W allow external devices to be designed independent of CPU timing constraints and considerations.

Miscellaneous Signals - Since the thrust of this analysis has primarily been to determine final form operating conditions, some of the ancillary functions have been deferred. These include control panel control, power contingencies, halting and clock control. These signals are unique to each particular CPU and as such have no system module counterparts.

Conclusions - The modifications required for the AN/UYK-30 necessary for inclusion into ONR Macro Modules are moderate. The fundamental CPU is retained while the I/O undergoes modification.

There is insufficient data to measure the full impact of the partitioning that has been recommended. Although superficially it appears minor, only detailed analysis can truly measure its full impact.

The details not withstanding the AN/UYK-30 appears to be an excellent candidate for inclusion into the macro-modular micro computer family.

5.2.3 Navy SAM/SEM Macro-Module Packaging

To utilize the AN/UYK-30 CPU as a high-speed 16-bit microprocessor module in the macro-modular micro computer family requires that the integrated-circuits (ICs) currently packaged on six Navy SEM-2A modules be consolidated in one Navy standard avionics module (SAM) or standard electronics module (SEM), using alternate low-power device technology and very large scale integration (VLSI) packaging techniques. Table 5.8 gives the IC counts and power dissipation of the existing AN/UYK-30 modules using Schottky-bipolar device technology. By comparison complimentary metal-oxide semiconductor, silicon-on-sapphire (CMOS-SOS) circuit implementation would achieve between 1/4 to 1/5 the power disinflation.

Reducing the total dissipation of the CPU to between 3.5 to 4.5 watts. This lower power dissipation would enable the whole CPU to be concentrated on one SAM or SEM-2A module using current 1000-gate array CMOS-SOS devices and hybrid packaging techniques. The configuration of the AN/UYK-30 CPU in macro-module form is shown in Figure 5.9.

TABLE 5.8

AN/UYK-30 CPU PACKAGING REQUIREMENTS

Module Name	Qty.	Total No. of I.Cs	Total Power Disinflation (Watts)
8-Bit RALU Slice	2	26	7.4
Timing and Control	1	22	2.0
Microprogram Memory	1	16	4.1
Counter Decoder	1	9	1.6
System and Interrupt Control	1	19	2.3
Totals:	6	92	17.4

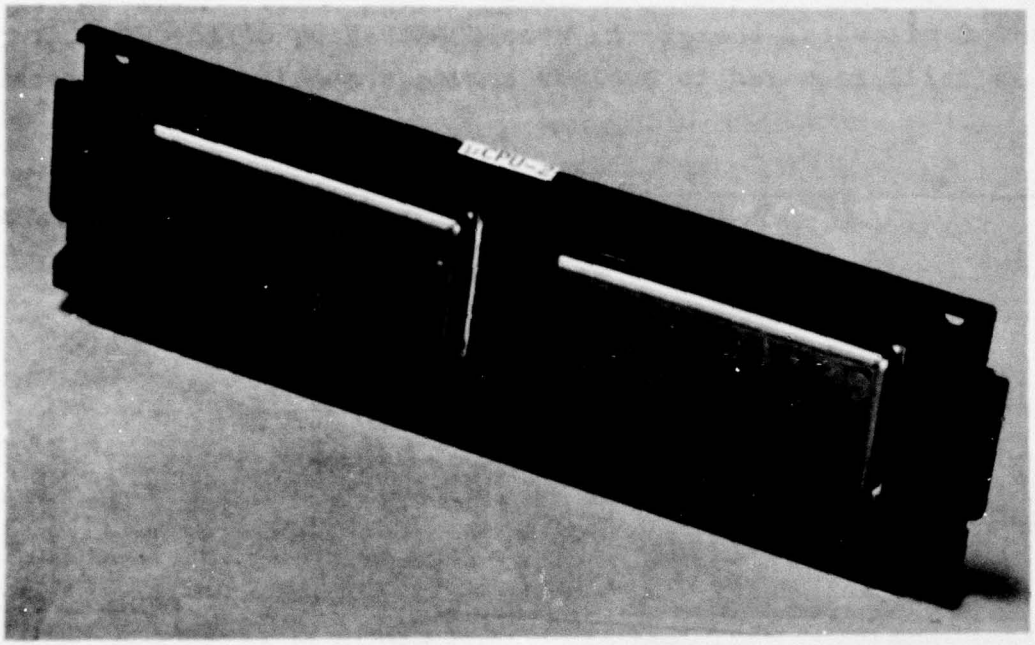


Figure 5.9 - AN/UYK-30 CPU as a Single SEM-2A Macro-Module

The two 8-bit slice RALUs are contained in one 2 in. x 1 in. hybrid LSI package, and the remaining microprogram memory and associated timing and control circuits are packaged in a second 2 in. x 1 in. hybrid. This approach is similar to that proposed in the Phase III Report (Ref. R-4).

The proposed Navy standard avionics module (SAM) Figure 5.10 is larger than the SEM-2A but is still limited to 30-36 integrated circuits, therefore, hybrid packaging of the CPU circuits is still required to achieve a single module configuration.

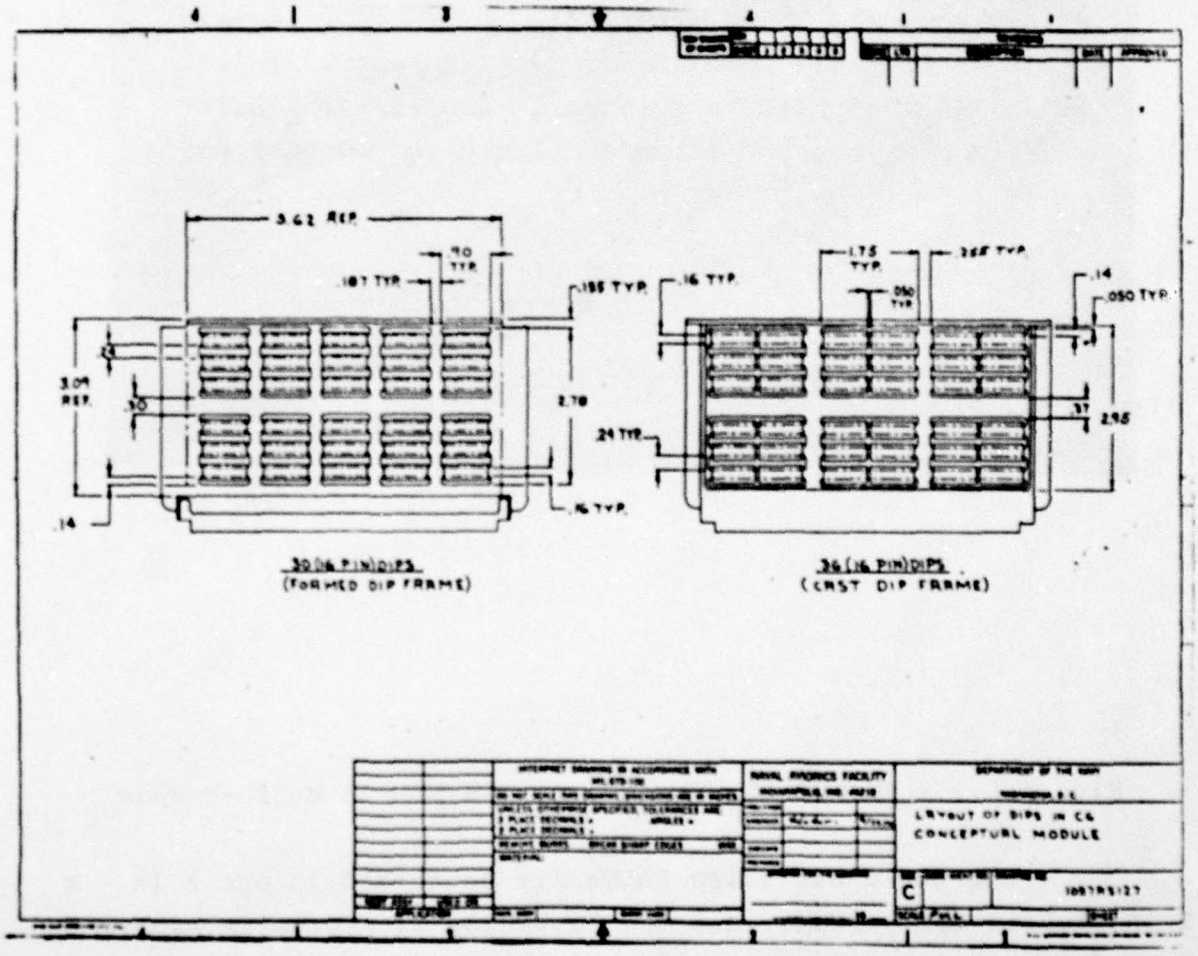


Figure 5.10 - Conceptual Design of Navy Standard Avionics Module

6. LOW-COST SERIAL DIGITAL INPUT-OUTPUT MODULE (SDIO)

Serial digital communication between microcomputers in distributed microcomputer systems can be costly in terms of the interface hardware required to drive conventional electrical busses. Nevertheless, the simplicity, reliability and lightweight attributes of a redundant single-wire interface remain attractive features for missiles. Furthermore, the use of the military standard serial digital multiplex interface (MIL-STD-1553A) provides compatibility with the aircraft avionics and associated ground support equipment.

To overcome the drawbacks of conventional electrical interface hardware, the use of fiber-optic data links was explored. It was found that presently available fiber-optic products, while influencing the form of communication network, (e.g. party-line, star, round-robin), offered significant size, weight, power and cost reductions compared to the electrical counterparts.

This task of the study was broken into the following three sub-tasks:

1) Review of available electrical interface circuits.
2) Review of available fiber-optic interface components.
3) Practical fiber-optic communication system.

6.1 Available Electrical Interface Circuits

Investigations showed that available electrical interface circuits were originally developed by several manufacturers for the Air Force B-1 strategic bomber program. To satisfy the conversion

from parallel to serial digital data and vice versa, the SDIO module is typically divided into three main sections (Figure 6.1).

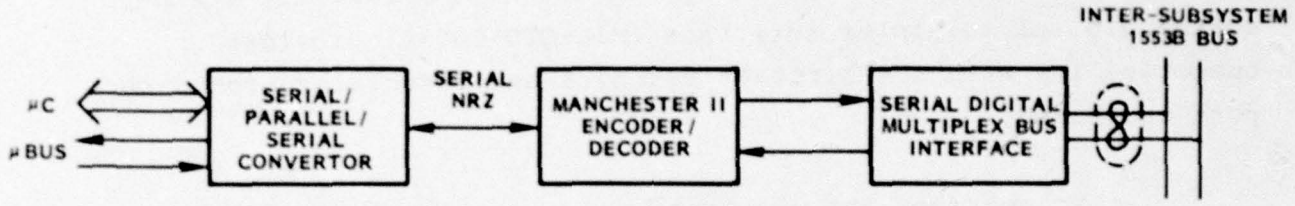


Figure 6.1 - Electrical Interface Circuits

6.1.1 Serial Digital Bus Interface

Since the MIL-STD-1553A specification (Reference R-14) calls for transformer coupling and fault isolation to a shielded-twisted-pair bus or stub for the serial-digital interface between subsystems, this interface is offered as an entity by some manufacturers (References R-15). Figure 6.2 illustrates one such available interface product. The power dissipation of the latter devices is relatively high, and contributes 99.5% of the total power dissipation of the entire SDIO module. Physically, these circuits are large, (Figure 6.3), which in turn conflicts with the size, weight and power limitations of small missile applications.

AD-A078 808 RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV F/G 17/7
MODULAR DIGITAL MISSILE GUIDANCE.(U)
DEC 79 F J LANGLEY , A J MANNION , K D LAUBE N00014-75-C-0549
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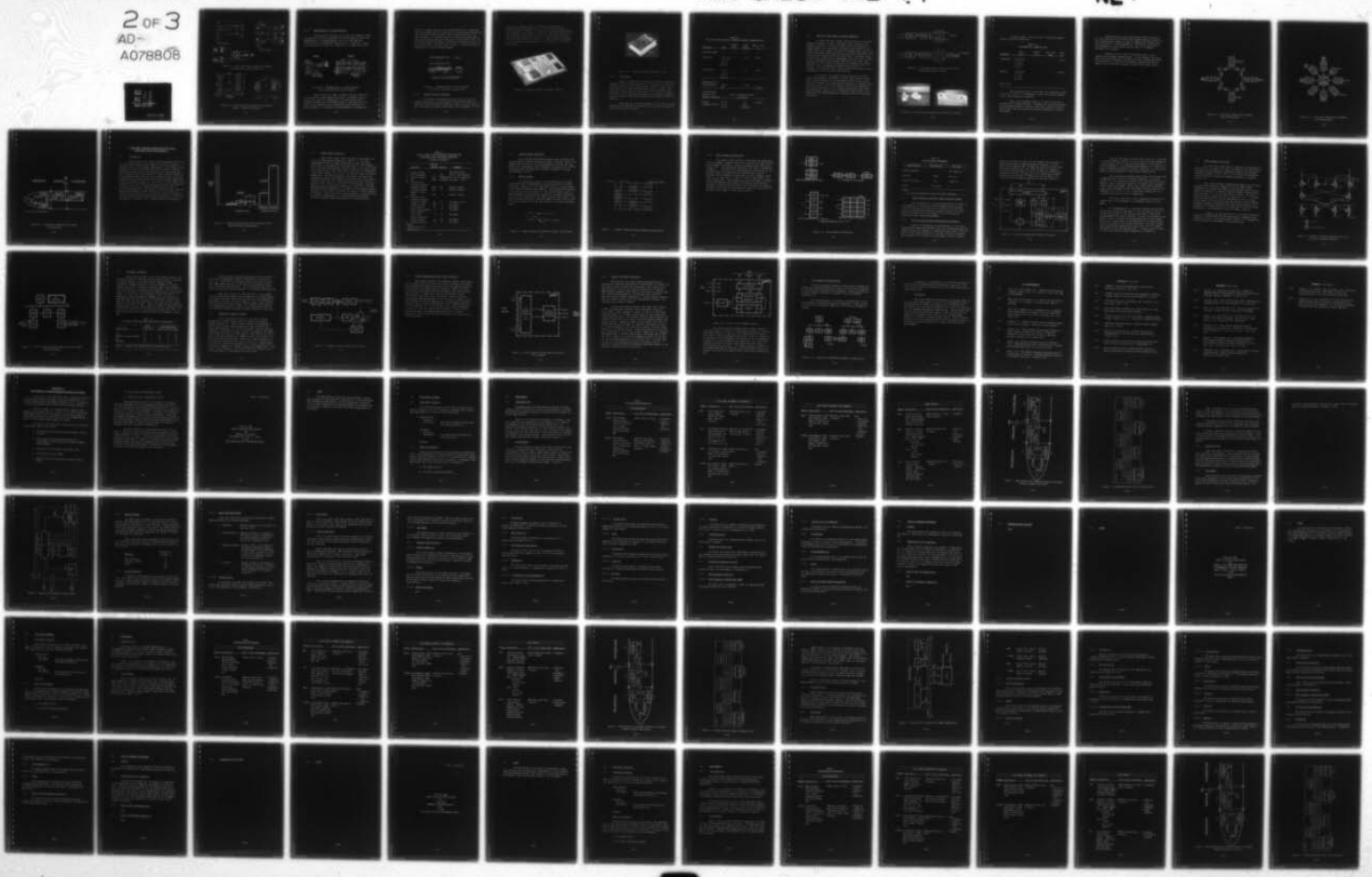

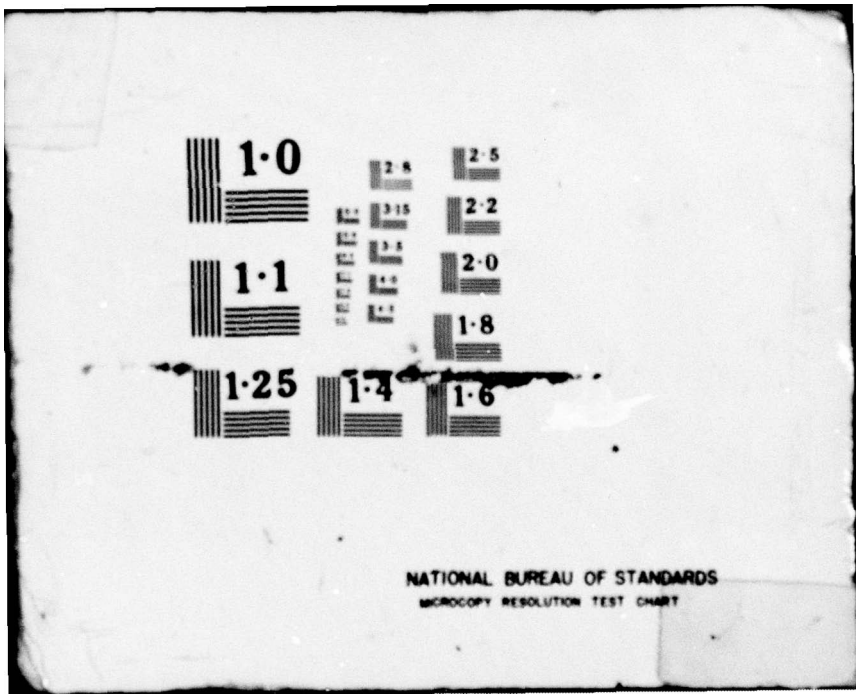
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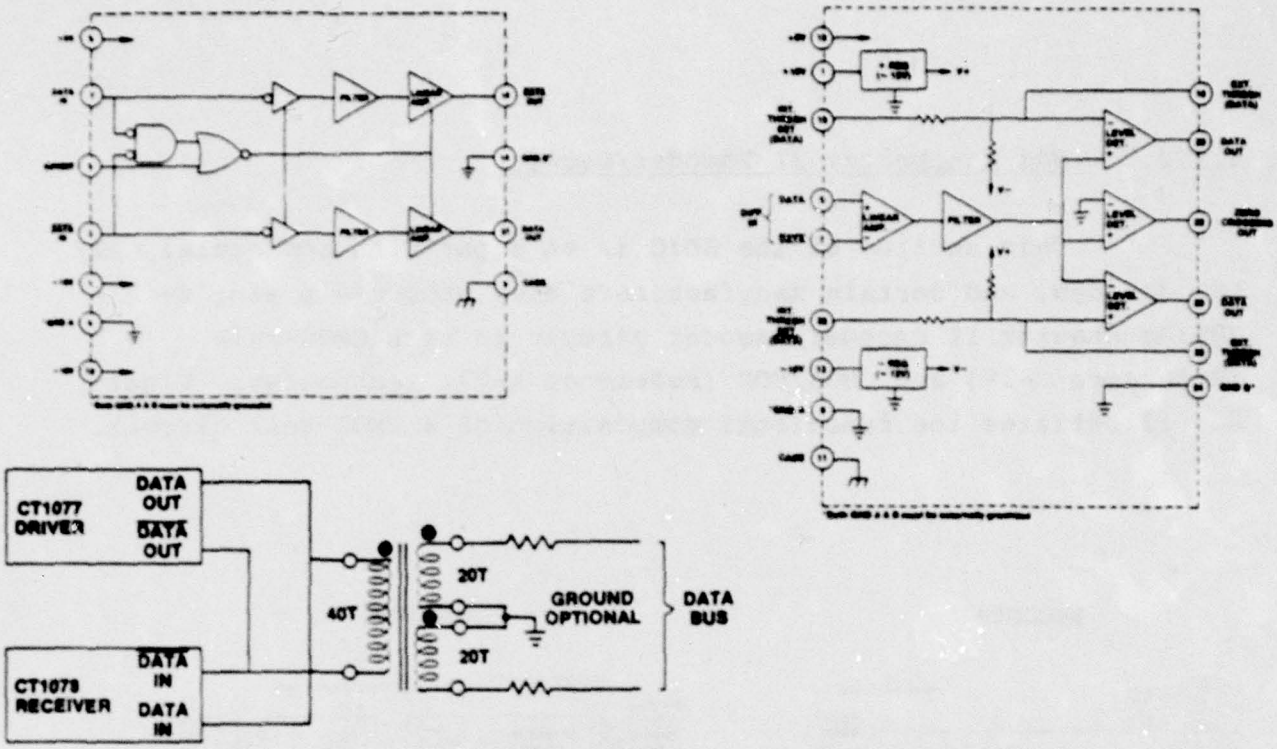


Figure 6.2 - Electrical Serial Digital Bus Diagram
Interface Module, Functional Block

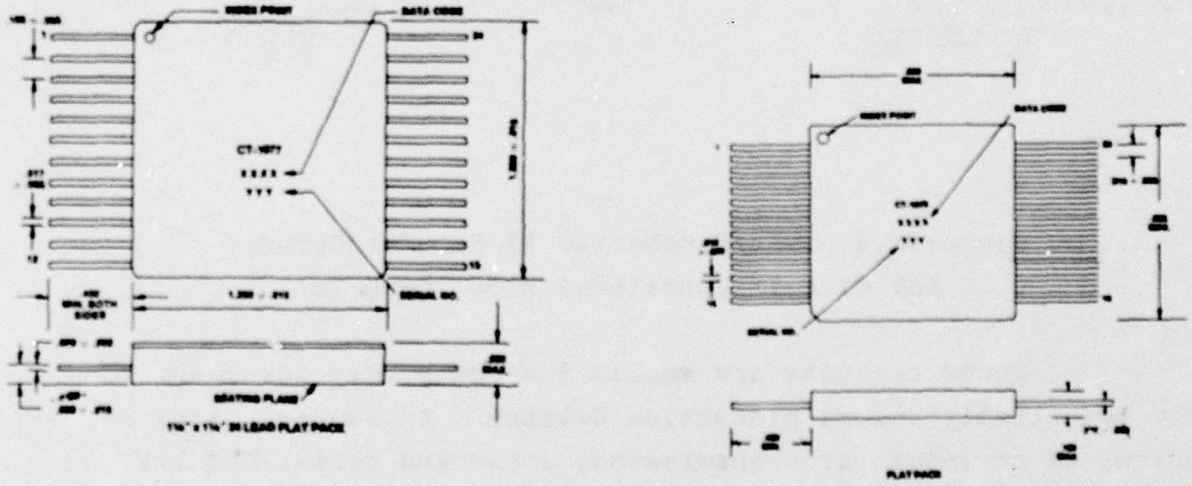


Figure 6.3 - Electrical Serial Digital Bus Interface
Module - Physical Dimensions

6.1.2 NRZ/Manchester II Encoder/Decoder

This section of the SDIO is on a par with commercial UART LSI devices, and certain manufacturers have produced a single-chip NRZ/Manchester II Encoder/Decoder circuit in both CMOS-bulk (Reference R-16) and CMOS/SOS (Reference R-17) technology. Figure 6.4 illustrates the functional composition of a CMOS-bulk circuit.

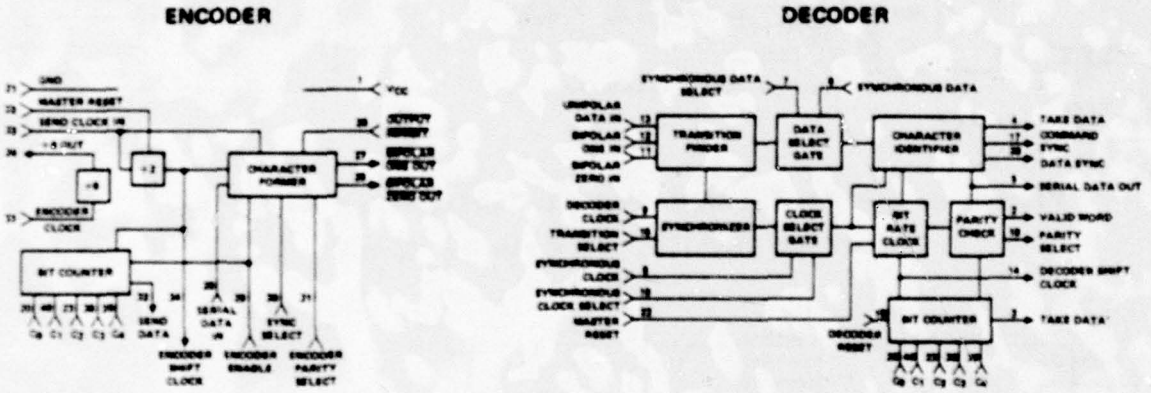
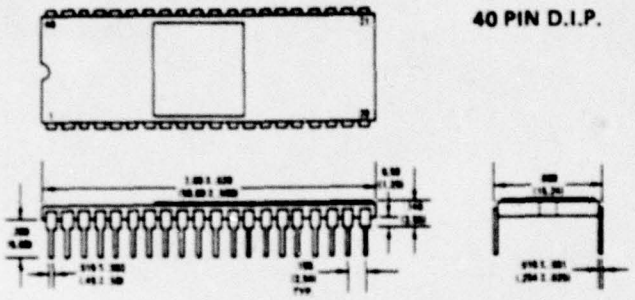


Figure 6.4 - NRZ/Manchester II Encoder/Decoder
LSI Circuit Functional Block Diagram

These circuits are small, dissipate very low power and are potentially volume production devices. In essence, they require, as an input for transmission, a clocked serial NRZ bit stream conforming with the message formats of MIL-STD-1553A, and then this is converted into an equivalent serial Manchester II output waveform. In reverse, a serial Manchester II message se-

quence is accepted from the line interface module and transformed into an equivalent NRZ bit stream with a "reconstructed" synchronous clock derived from the waveform. All interface levels are T^2L logic voltages. In addition parity error checking is performed on chip and the status indicated along with the serial NRZ output. As such, these single chip devices constitute the remaining portion of the RTU described in MIL-STD-1553A. Figure 6.5 shows the physical dimensions of a typical encoder/decoder.



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±.025mm) unless otherwise shown.

Figure 6.5 - NRZ/Manchester II Encoder/Decoder
LSI Circuit, Physical Characteristics

6.1.3 Parallel Digital Interface

The computer interface constitutes the only non-1553A standard portion of the serial digital input-output module and therefore few manufacturers provide this since it can vary according to the specific computer being used in the subsystem. At best,

this can be a generalized form of 16-bit parallel digital interface with the necessary control lines to transfer data to/from a computer I/O channel. A review of available products showed this interface to be provided as part of a composite serial I/O module by one system house (Figure 6.7), while another provides a serial NRZ data interface (Figure 6.6). The formation of message words is assumed to be made external to the module, i.e., within the computer.

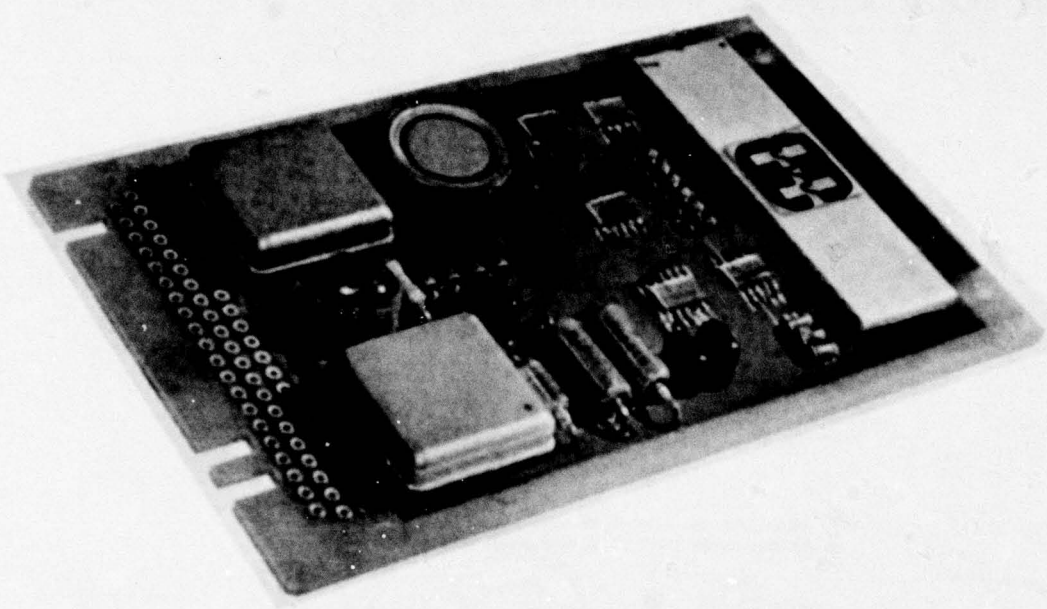


Figure 6.6 - Composite Serial I/O Module, (Harris)

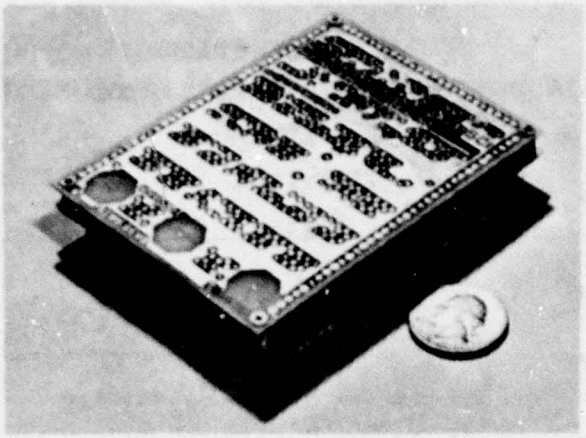


Figure 6.7 - Composite Serial I/O Module, (SCI)

6.1.4 Conclusions

Table 6.1 summarizes the electrical and cost aspects of available 1553A interface products. It can be seen that the line interface section is the chief problem in terms of size, weight, power and cost for small federated microcomputer systems. The remaining circuits could be fabricated as two separate low-power LSI chips, one of these being already available, and the parallel digital interface could become standard when designed to match the ONR μBus.

Based upon the latter observations, fiber-optic interface components were explored to achieve a more practical interface for missile microcomputer systems.

TABLE 6.1

MIL-STD-1553A ELECTRICAL INTERFACE PRODUCT CHARACTERISTICS

Component	Size	Weight (ozs.)	Power (Watts)	Approx. Cost ($)
Bus Transformer	-	-	-	-
Bus Driver	1.25 in X 1.25 in X 0.2 in Hybrid	-	3.6	180.00
Bus Receiver	1 in X 1 in X 0.15 in Hybrid	-	1.5	120.00
NR2/Manchester II Encoder/Decoder	24-Pin DIP	-	0.025	165.00
Serial/Parallel Convertor and Computer Interface	- - - Part of complete module - - - (see below)			
Totals: (Complete Module)	4 in X 3 in X 0.4 in		4.5 max. (transmit)	1,500.00

6.2 Available Fiber-Optic Interface Components

To reduce the size, weight, power and cost of the serial digital interface, a survey of available fiber-optic data link components was made. During the course of this investigation it became apparent that the modest performance requirements of short digital links with 1 mega bit per second (IMb/sec) data rates could be satisfied with simple fiber-optic, wire-bundle type cables terminated with PIN diode receivers and LED drivers. The major thrust in fiber-optic communications development was found to be in common carrier telecommunications systems (Reference R-18) where 2GHz bandwidths for low distortion analog data transmission was being achieved. Such developments provided higher density (no. of channels) over existing routes thereby offsetting the ever increasing demand for more voice and video channels.

In contrast, the simple terminals required for short-length, medium-speed, (DC-2Mb/sec), digital data links has given rise to the availability of DIP-packaged T^2L/fiber-optic coupler. The latter enables the serial-digital (Manchester II encoder) input and output parts of the encoder/decoder LSI circuit, described in the previous subsection, to be coupled directly with there fiber optic terminals. Figure 6.7 illustrates the substitution of the electrical transformer-coupled bus interface with the fiber-optic counterpart.

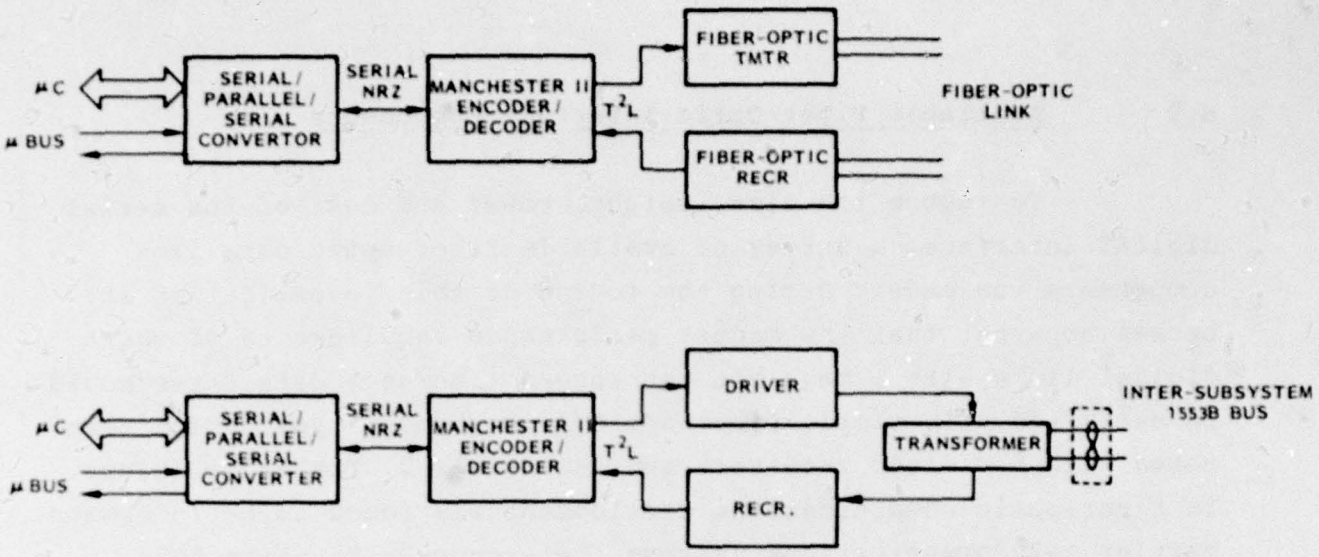


Figure 6.7 - Fiber-Optic Bus Interface Vs Electrical Transformer-Coupled Interface

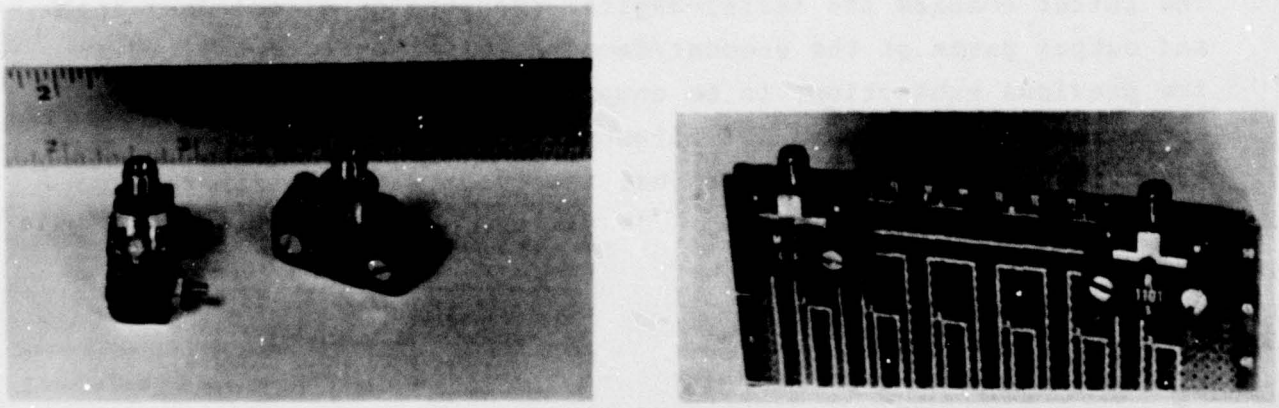


Figure 6.8 - Available Fiber-Optic/T^2L Terminal Units (Meret)

The size, weight, power and cost of these DIP-packaged devices is given in Table 6.2.

TABLE 6.2

T^2L/FIBER-OPTIC TERMINAL UNITS

Terminal	Size (ins.)	Weight (ozs.)	Power Diss. (mW)	*Cost ($)
Transmitter	14-pin DIP (1 in X 0.5 in X 0.4 in)	-	-	54.00
Receiver	14-pin DIP (1 in X 0.5 in X 0.4 in)	-	-	180.00

*Qty: 10-24

From the above data it can be seen that significant reductions in the values of the parameters listed are possible compared to the former electrical interface.

There is one drawback, however, in terms of the use of T-couplers for a party-line bus. T-couplers are currently unavailable as standard products. Further, they have a typical insertion loss of 3dB, such that signals are heavily attenuated in a multi-tap system.

Alternatively, the Air Force has sponsored the development and fabrication of an 8-port star coupler (Reference R-19, but this automatically changes the type of communication system from a party-line bus to a star mechanization. The latter item requires one subsystem to be the central control point or "telephone exchange" of the system.

Figures 6.9, 6.10, and 6.11 show the three forms of communication systems discussed above. In this respect, the available fiber-optic components influence the type of communication system practicable for federated microcomputer guidance and control, namely: ring (round-robin protocol) or star with central control.

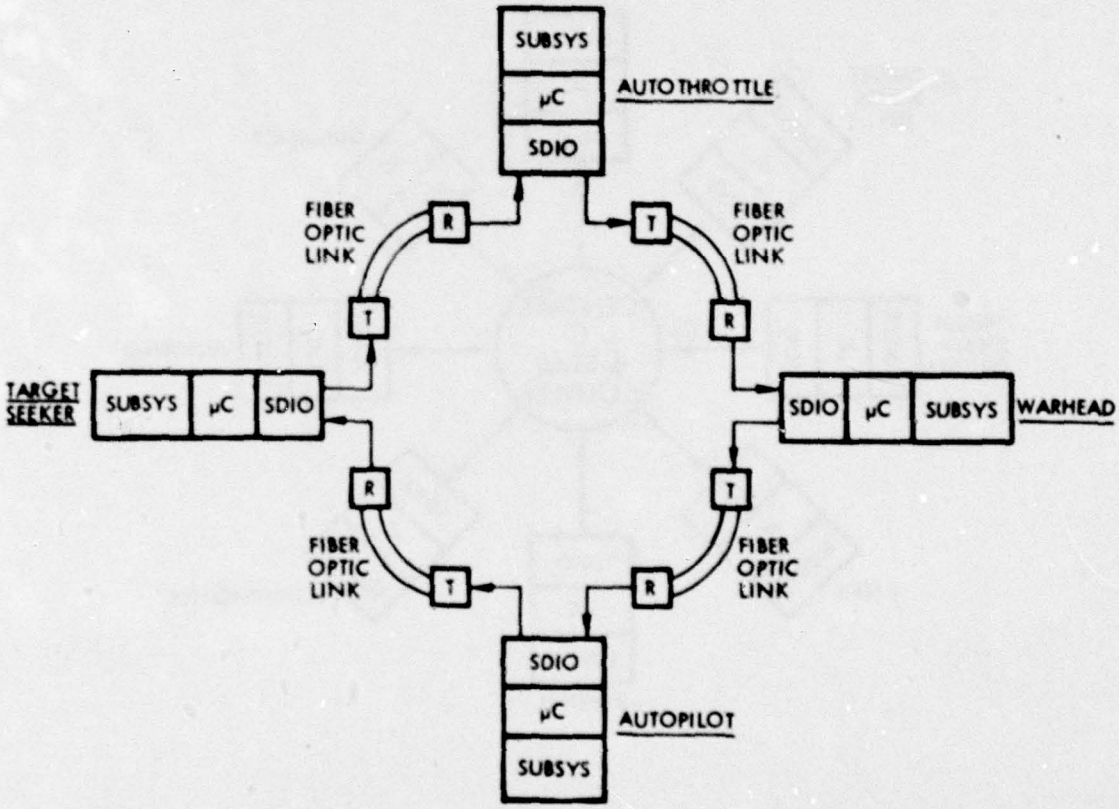


Figure 6.9 - Fiber-Optic Communication Systems
Ring Configuration

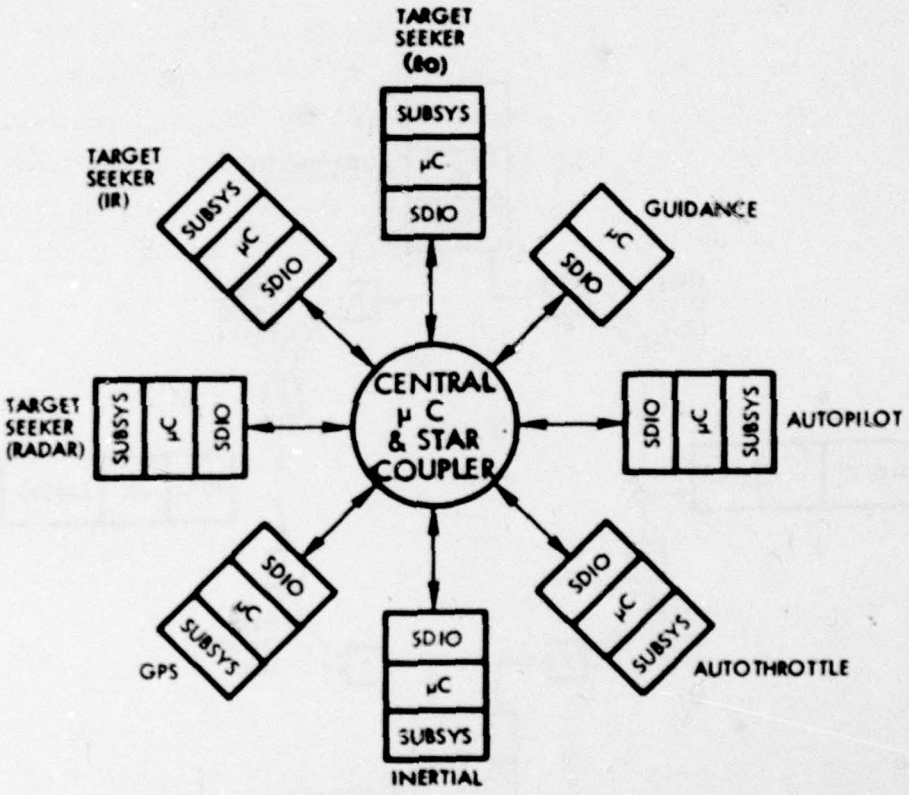


Figure 6.10 - Fiber-Optic Communication Systems, Star Configuration

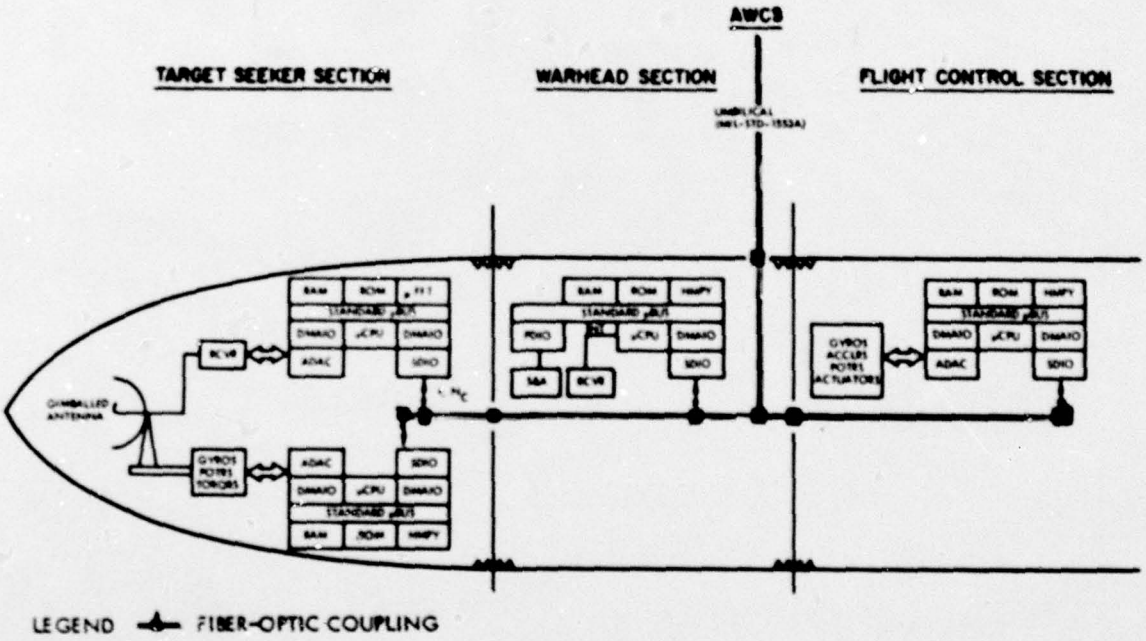


Figure 6.11 - Fiber-Optic Communication Systems, Party-Line Bus

7. LOW-COST, CHARGE-COUPLED DEVICE (CCD) SPECTRUM ANALYZER MODULE

7.1 Introduction

While missile radar sensor signal processing constitutes the worst case processing load compared to angle-only electro-optical sensors, the throughput requirements of the former are low compared to avionic and ground-based tactical radars, (Figure 7.1). Despite the relative size of the missile signal processing task, the integrated circuit requirements for such a microbus signal processing module exceed those of the host microprocessor by an order of magnitude with proportionate size, weight and power penalties. With this top-heavy situation in the context of today's small microprocessor world, alternative LSI device technologies were explored to shrink the size of the signal processing module without sacrificing performance. This section reviews the radar signal processing requirements in terms of functions to be executed and overall timing constraints to meet the performance of the missile, and then relates state-of-the-art device technologies to the latter requirements to determine their respective merits and demerits.

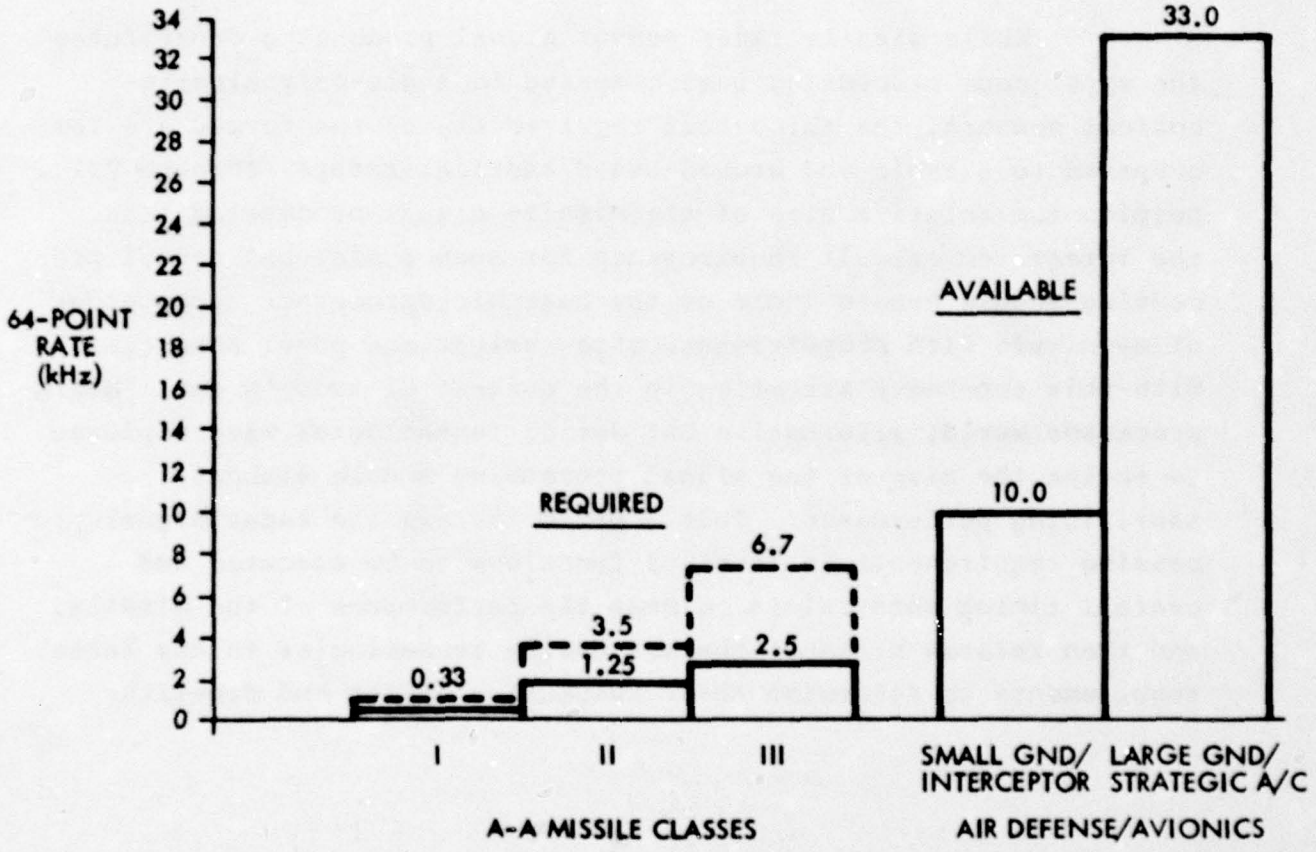


Figure 7.1 - Missile versus Avionic and Ground-Based Radar Spectrum Analysis Requirements

7.2 Radar Signal Processing

Radar target seeker signal processing requirements for air-to-air missiles are summarized in Table 7.1. The high-performance drivers of signal processing are the pulse-doppler radars used in the medium and long-range Class II and III missiles, due to the multi-range doppler matrices formed during target acquisition and the short time (dwell time) allowed for the processing of the radar returns, (i.e., 5 ms). Of the seven major functional components of the signal processing chain shown, the most time consuming in digital technology are the Cooley-Tukey fast Fourier transform (FFT), Ref. R-20, spectrum analysis and post detection integration (PDI) functions, since these are performed on all data samples during the acquisition phase and, in the case of the FFT, $2N\log_2 N$ multiply operations are involved for each monopulse channel processed in each range bin (N being the number of complex samples per channel). Thus, the latter functions present an excessive load for software implementation by a medium-speed microcomputer, forcing a hardware/firmware mechanization of these functions.

TABLE 7.1

MISSILE RADAR SIGNAL PROCESSING FUNCTIONS AND ASSOCIATED DATA PROCESSING OPERATIONS (CLASS III MISSILE)

	FUNCTION	ADD/SUB LOGICAL	MPY/DIV	COMMENTS
1.	Corner Turning	-	-	Data Reordering
2.	Cos^2 Weighting	0	128	Per ch. and range bin
3.	FFT (64-complex)	1152	768(mpys)	Per ch. and range bin
*4.	PDI	2560	640(divs)	Per dwell (5 ms)
*5.	Threshold and Detection Sliding threshold detect	4500	500	Every 10 dwells
	Mainlobe clutter	1320	0	Every 10 dwells
	Jammer to noise ratio	501	3	Every 10 dwells
**6.	Threshold and Detection Sliding threshold detect	450	50	Per dwell (Σ ch.)
	Jammer to noise	501	3	Per dwell
	Beta blanking	13	8	Per dwell
	Radial angle gating	6	4	Per dwell
	Track quality indication	2	12	Per dwell
	Angle, range and doppler errors	34	28	Per dwell
**7.	Target Selection	48	0	Per dwell

Notes

*Acquisition only

**Track only

7.3 Digital Signal Processing

Since the FFT constitutes the major task in digital signal processing, attention has been focussed on efficient ways to implement this function as a first consideration with PDI and other second order throughput drivers addressed as adaptations to the FFT processor either by adding more arithmetic elements or control microprograms, or both.

7.3.1 FFT Processing

To recapitulate briefly on the mechanism of the Cooley-Tukey algorithm, it fundamentally involves executing a two-point transform. (Figure 7.2), $N/2 \log_2 N$ times where N, a binary number, is the number of complex input samples. The complete FFT algorithm is of the form shown in Figure 7.3. The primary design goal for FFT processors is to execute $N/2 \log_2 N$ basic two-point transforms within the time allowed for the complete N-point FFT, which, in the case of Class II air-to-air missiles ranges from 300 to 800 μs, and for Class III types 150 to 400 μs, based on the 64-point benchmark value.

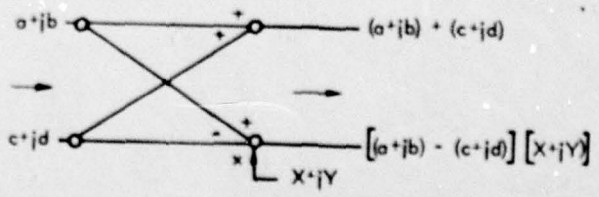


Figure 7.2 - Basic Two-Point Transform Arithmetic and Data Flow

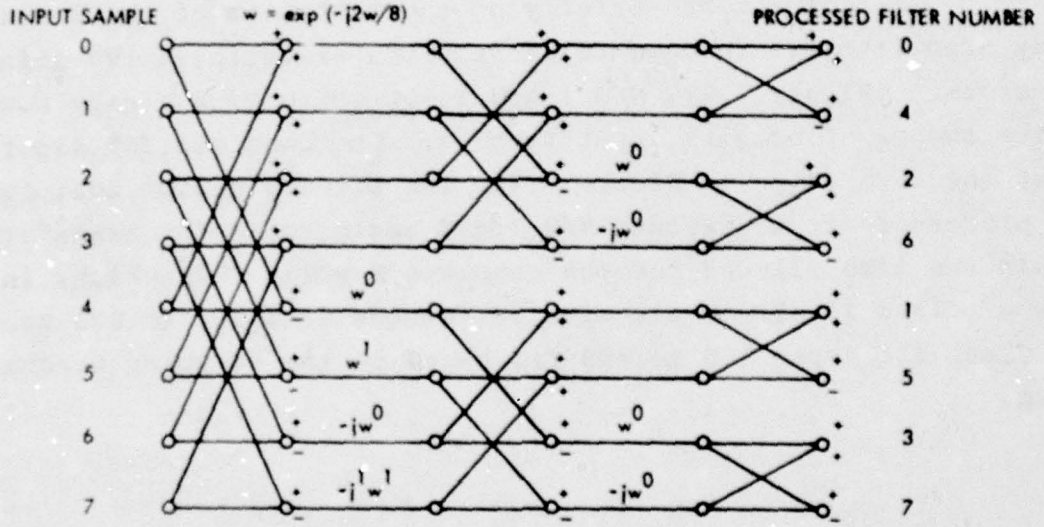


Figure 7.3 - Complete Eight-Point FFT Arithmetic and Data Flow

7.3.2 FFT Processor Architectures

Four types of FFT processor architecture are significant from a throughput viewpoint, Ref. R-21, and these are characterized by the number of two-point transform arithmetic units (AUs) used, (Figure 7.4). The performance obtainable from these is summarized in Table 7.2. Selecting the single sequential architecture as the minimum hardware configuration for missiles means that the processor must be capable of executing a two-point complex transform in 1.6 s max and 0.8 s max for Class II and Class III missiles respectively. These speeds are quite practicable in current bipolar and CMOS/SOS semi-conductor technology using multiple arithmetic elements pipelined within the AU together with parallel addressing techniques to simultaneously access and return pairs of operands from/to memory at each clock interval.

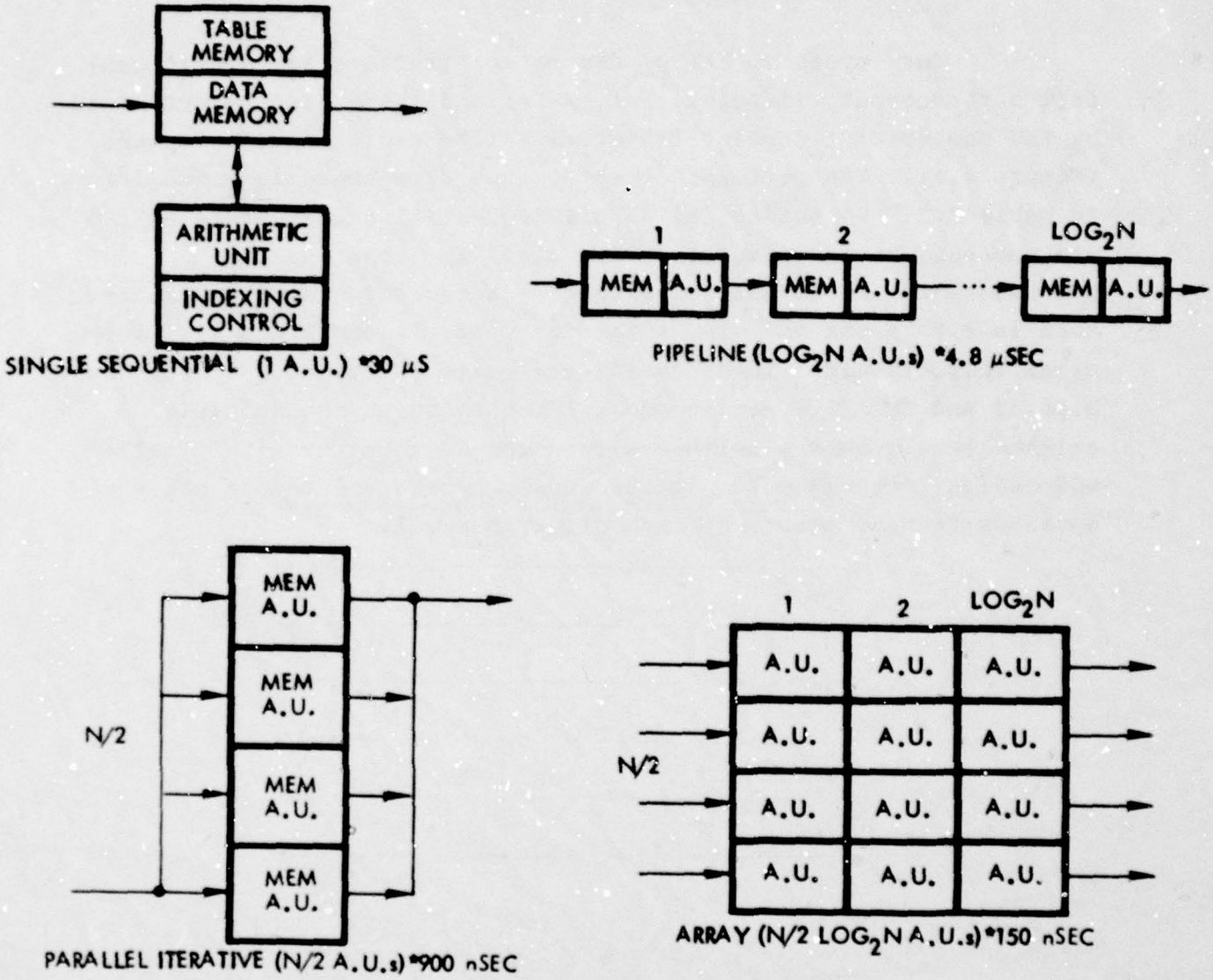


Figure 7.4 - FFT Processor Architectures

TABLE 7.2
FFT PROCESSOR PERFORMANCE

ARCHITECTURE	TWO-POINT AUs	FFT TIME
Single Sequential	1	$N/2 \log_2 N \times B$
Pipeline	$\text{Log}_2 N$	$N/2 \times B$
Parallel Iterative	N/2	$\text{Log}_2 N \times B$
Array	$N/2 \log_2 N$	B

Notes:
B - Time to execute the basic two-point transform

7.4 Single Sequential Digital Signal Processors (DSPs)

The architecture of single sequential DSPs is similar in many respects to conventional microprogrammed general-purpose processors except for the provision of extensive internal data buffering and pipelined hardware arithmetic elements to achieve higher throughput, as will be apparent from the processors described in the following paragraphs.

7.4.1 Bit-Slice Microprocessor-Based Signal Processors

Figure 7.5 illustrates the architecture of a bit-slice microprocessor-based FFT processor using two random-access memories (RAMs) to store the sequence of complex data pairs used in the execution of $N/2 \log_2 N$ iterations of the basic two-point transform. The arithmetic unit consists of a high-speed, (220 ns), hardware

multiplier followed by three 4-bit slice (Am2901) microprocessor elements which provide the add and substract functions. A coefficient read-only memory (ROM) furnishes the complex multiplier terms and a micro program control unit (μPCU) contains the sequence of microinstructions necessary to control the fetching of operands via the memory controller, the execution of the appropriate arithmetic operations and the storage of results back into the RAMs in the correct order for subsequent iterations of the basic operation.

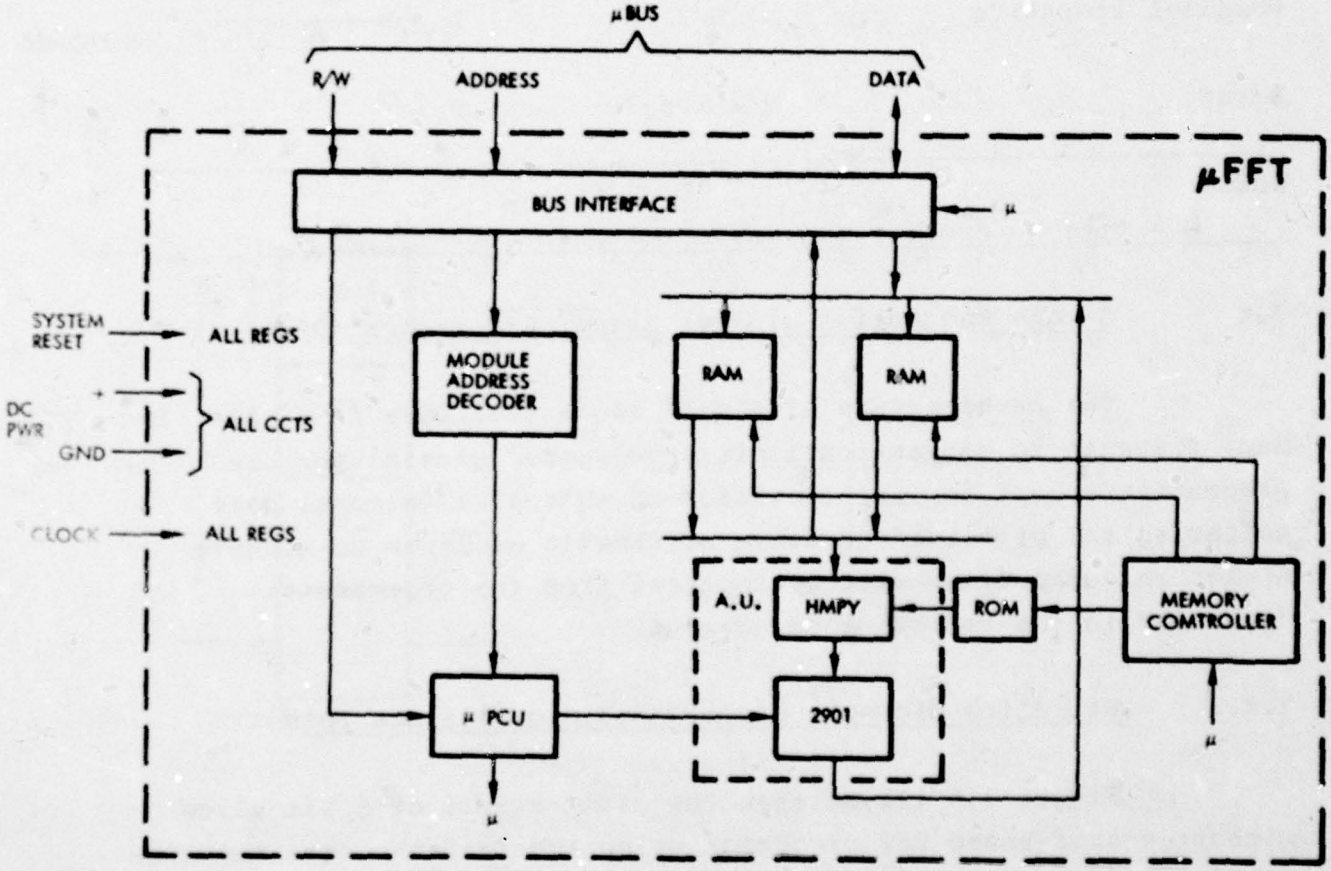


Figure 7.5 - Bit-Slice Microprocessor-Based FFT Processor

Such an architecture has been shown, Ref. R-4, to execute a two-point complex transform in 1.6 μs, and a 64-point complex FFT in approximately 300 μs; requires approximately 150 LSI/MSI/SSI circuits to mechanize, and dissipates approximately 50 W. While this meets the speed requirements of Class II missiles, the physical parameters are unacceptable for small missile applications.

One alternative low-power semiconductor device technology is CMOS/SOS, Ref. R-22 which although comparable to Schottky-bipolar in circuit density and parts count, nonetheless provides at least an order of magnitude reduction in dynamic power dissipation, without sacrificing speed. Hence, very-large-scale-integration (VLSI) hybrid packaging of the FFT module could be achieved with CMOS/SOS, e.g., two 2 in. x 1 in. hybrid-LSI packages for the arithmetic and control sections respectively.

The other alternative circuit implementation would be in digital CCDs, to be discussed in a subsequent section of this paper.

To accommodate PDI in the above processor architecture would require duplicate RAM space to store the spectral values resulting from the FFT of the previous radar dwell. Additional microprograms would also be required to control the arithmetic elements in order to compute the modules/magnitude of each complex value and to average each filter magnitude with successive dwell values in accordance with the PDI algorithm. The latter process would require more sophisticated control than that of a system tailored to do just the FFT algorithm. In other words the trade-off for a more general-purpose capability is complexity.

7.4.2 Higher-Speed Two-Point AU

For the longer range Class III missiles with typically 10 range bins for the acquisition mode, the speed of the single sequential DSP can be increased by progressively adding more discrete arithmetic elements in the AU until a 1:1 hardware correspondence with the two-point transform arithmetic operations is achieved, (Figure 7.6).

Such a fully parallel, pipelined arithmetic unit with appropriate data buffering, supported by the two RAMs, memory addressing unit, coefficient ROM and microprogram control unit, is capable of outputting a complete two-point complex transform every clock interval, i.e., 150 ns with bipolar circuits. The corresponding 64-point complex FFT time is less than 30 μs. To satisfy the worst case Class III missile requirements of 150 μs, a one-fourth reduction in parallelism and time sharing of the arithmetic elements increases the benchmark FFT time to approximately 115 μs. Hardware cost is approximately 450 LSI/MSI/SSI circuits with power dissipation in the hundreds of watts for bipolar circuits.

In summary, the high parts count of the above minimum configuration, single sequential DSP architectures, compared to the single-chip, 16-bit, host microprocessor (Figure 7.7), prompted the following review and assessment of CCD alternatives.

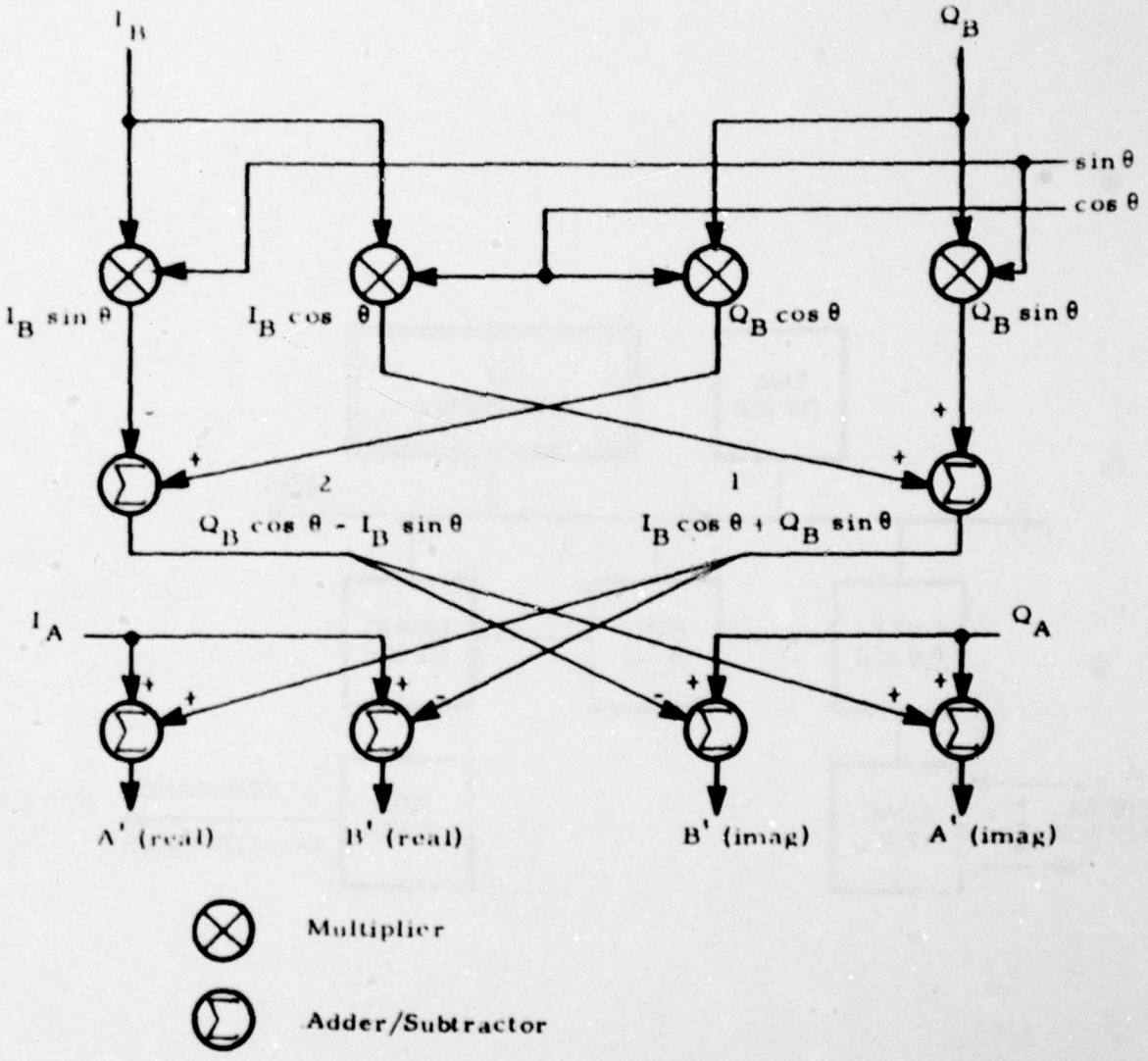


Figure 7.6 - Complete Arithmetic Representation of a Two-Point Transform Algorithm

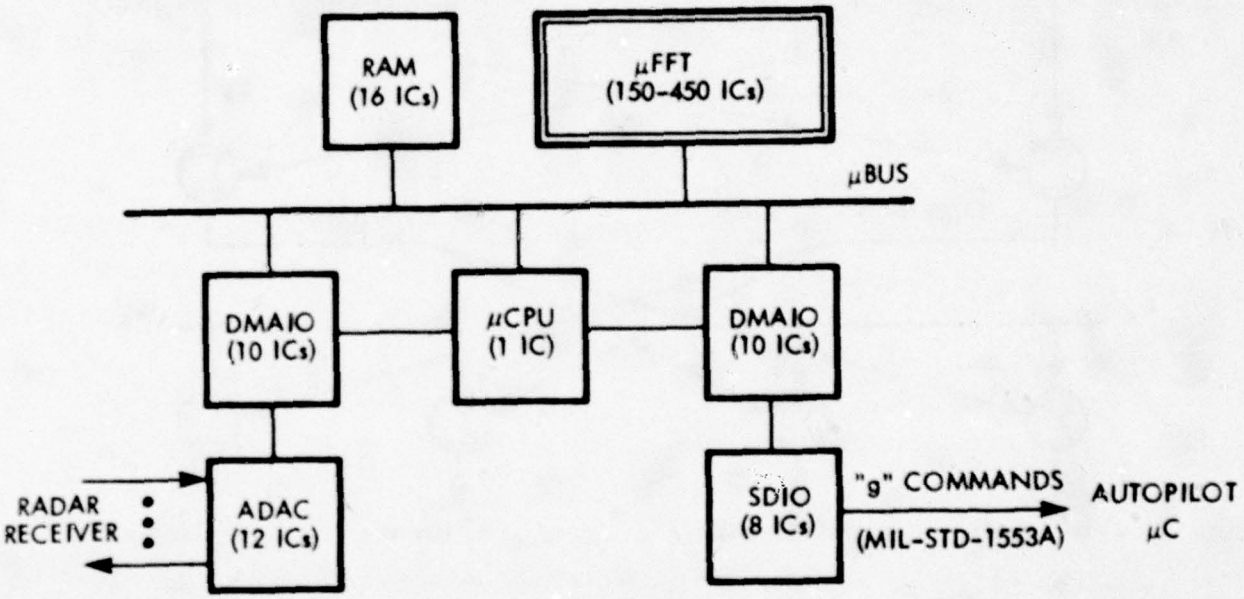


Figure 7.7 - Current Digital Signal Processor IC Counts versus Host Microcomputer

7.5 CCD Signal Processors

Analog CCDs have been in use in one form or another over the past five years in applications where data storage is required for short intervals, e.g., photo-optical imaging, display refreshing. Refresh intervals of 30 ms are common in the photo-optical field, which is similar to missile radar sensor applications where dwell or looking periods of between 5 and 20 ms are the norm. In the context of other existing semiconductor technologies, (Table 7.3), Ref. R-23, when projected to 1980, CCDs can be expected to provide the speed of CMOS/SOS for up to one-half the power and one-tenth the chip area, notwithstanding liberal allowances for power and size reductions in the latter and other candidates over the next two years. Hence, for pipeline-type signal processing tasks, at least, CCDs potentially have the necessary characteristics for single-chip, very-large-scale-integration (VLSI), to match the density of the random-processing, microcomputer counterpart.

TABLE 7.3

CCD VERSUS OTHER CANDIDATE SEMICONDUCTOR TECHNOLOGIES

	GATES		SHIFT REGISTERS		
CIRCUIT TYPE	(PJ)	Mil^2	W/bit	Mil^2/bit	MHz
CCD	0.2	2	1	0.5	50
Bipolar (Triple-Diffused)	3.0	5	100	8	100
I^2L	0.2	2	20	3	5
CMOS/SOS	0.2	3	2	5	50

Notes: Projected 1980 Characteristics, All Technologies

Three CCD signal processor mechanizations are reviewed in the following paragraphs, based on developments in the field to date, viz: analog chirp Z-transform (CZT) using surface acoustic wave (SAW) delay line filters, CZT with CCD transversal filters, and an all-digital FFT processor. The CZT algorithm, Ref. R-24, being the practical analog counterpart to the digital FFT algorithm.

While dark current is a limiting factor in the dynamic range of analog CZT processors at the upper end of the MIL temperature range, (typically 100 ms saturation time at room temperature, decreasing by a factor of two for every 8°C rise), recent improvements in prototype surface channel CCDs at Raytheon have achieved room temperature saturation times of 1 s, and periods as high as 20 s have been recently reported by Belgian researchers, Ref. R-25.

7.5.1 CZT/SAW Line Signal Processor

A fully operational version of this form of analog, sampled-data, signal processor has been recently developed at Raytheon (Figure 7.8). This processor employs 148 components to perform multi-channel spectrum analysis, target detection and output data buffering. Six of the total parts count are standard commercial, buried-channel, CCDs, used for the sampling, and temporary storage (5-20 ms), of radar receiver video outputs, and the selection and time compression of samples to match the duration of a SAW line generated chirp pulse. While not a viable candidate for low-chip-count, monolithic VLSI, with 5 and 10 in. long SAW lines, the processor executes the equivalent of a 64-point complex FFT in 30 μs, for a modest 24 W. Dynamic range at room temperature is limited to 30 dB, compared to the 72 dB of digital processors, but a 10 dB improvement is anticipated with future CCDs.

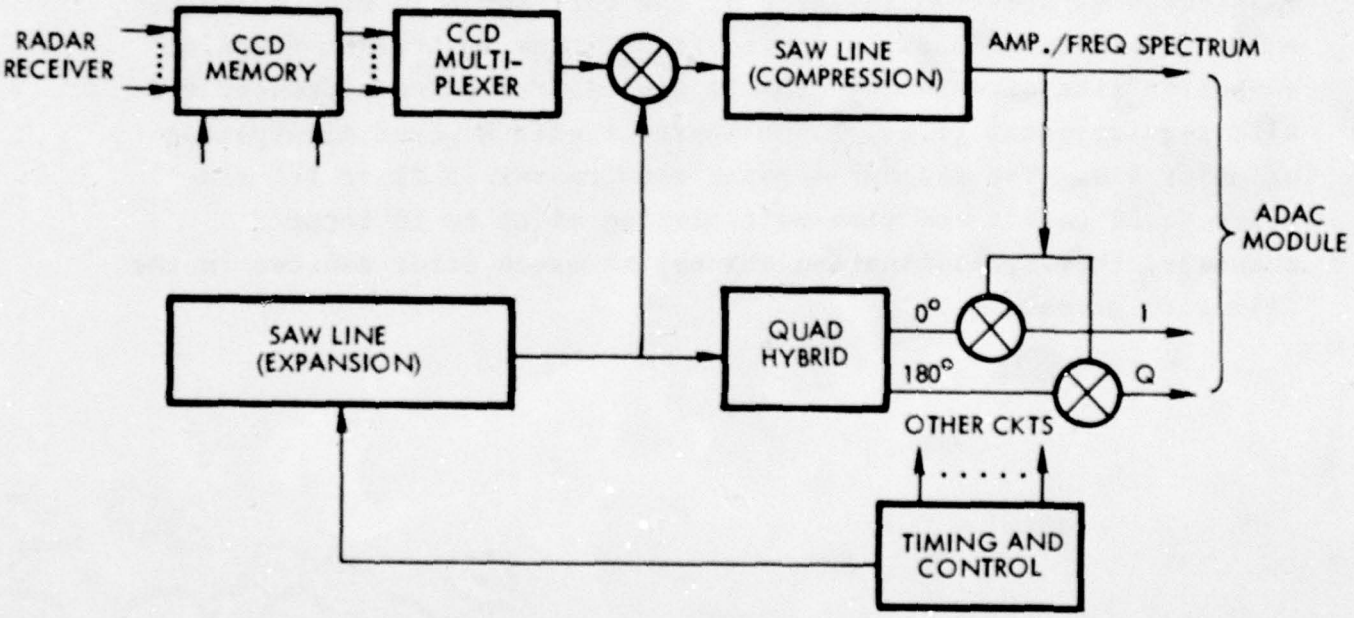


Figure 7.8 - CZT/SAW Line Signal Processor Block Diagram

7.5.2 CZT/CCD Transversal Filter Signal Processor

Apart from the present but temporary dynamic range limitation of analog CCDs for missile radar signal processing, the speed, packing density and power dissipation of CCD CZT spectrum analyzers are attractive for fixed function processing. Based on the work currently being performed by Texas Instruments under NASA and Army ECOM contracts, a single-chip, 64-point CZT processor can be realistically predicted in the near future. Hence a two-chip, multi-channel spectrum analyzer of the form shown in Figure 7.9 becomes feasible for missile applications. The equivalent 64-point execution time of existing CCD/CZT devices far exceeds present missile requirements, (i.e., 13 μs approx.) with a power dissipation of under 5 W. The 150 μs/64-point requirement of Class III missiles would permit the time-multiplexing of up to 10 input channels, thereby eliminating channel mismatch error sources in the filtering process.

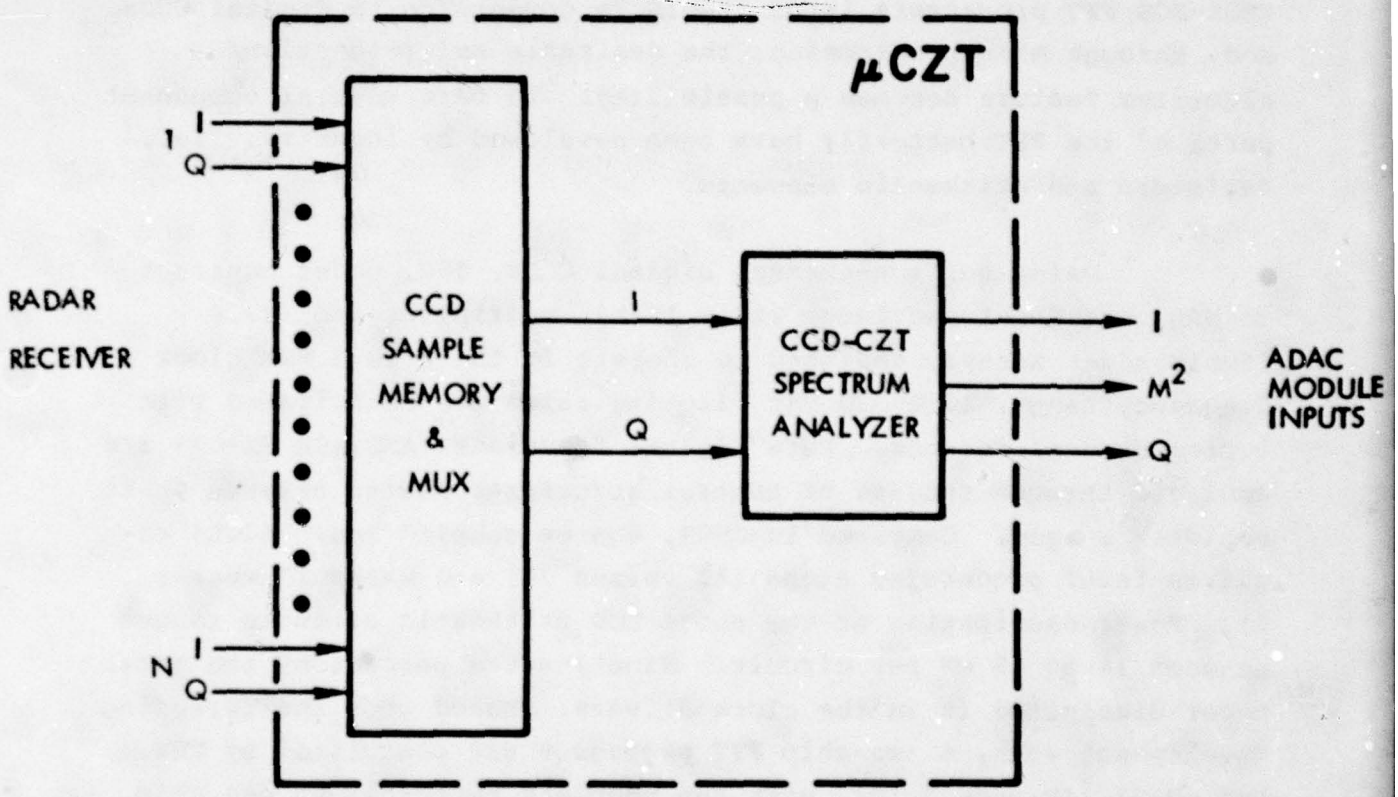


Figure 7.9 - Multi-Channel CCD/CZT Spectrum Analyzer, Block Diagram

7.5.3 Digital CCD Signal Processors

By using only two charge states and maintaining the clocked shift-register mechanization of analog CCDs, the digital domain offers virtual freedom from the dynamic range limitations of analog systems. Further, the pipeline architecture of bipolar/CMOS-SOS FFT processors lends itself to conversion to digital CCDs, and, through microprogramming, the desirable multi-function/algorithm feature becomes a possibility. To date several component parts of the FFT butterfly have been developed by industry, i.e., registers and arithmetic elements.

Using surface-channel digital CCDs, TRW, under contract to NRL, has developed large 8x8 = 16-bit multiplier and 16+16 = 16-bit adder arrays, designed to operate in the 2 to 5 MHz clock frequency range. 10 to 20 MHz clocking rates are anticipated with buried-channel devices. Pure logical functions (AND, OR EX-OR) are achieved through the use of control structures placed between shift register stages. Compared to CMOS, charge-coupled logic (CCL) requires fewer processing steps (12 versus 20) and masks (5 versus 8). Power dissipation of the above CCD arithmetic circuits ranges between 14 to 15 mW per circuit. Ninety-seven percent of the total power dissipated is in the clock drivers. Based upon the foregoing development work, a two-chip FFT processor was postulated by TRW, Ref. R-23, (Figure 7.10), with the complete butterfly on one chip and the data memory/sequencer on the second chip. A microprogram control unit with appropriate butterfly interfaces would be required to execute additional processing algorithms subject to the degree of flexibility built into the AU.

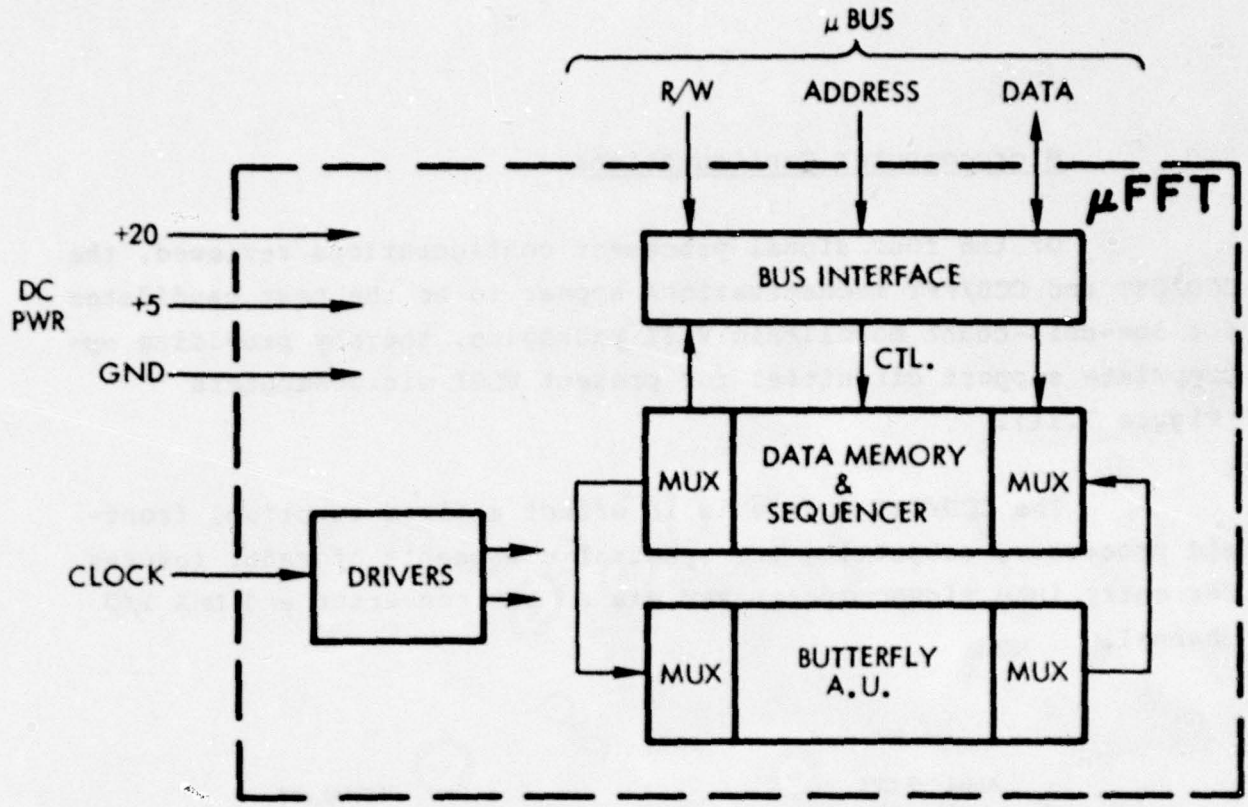


Figure 7.10 - Two-Chip VLSI CCD/FFT Processor

One significant fact emerges from this VLSI butterfly-on-a-chip, namely the number of input-output connections. Two 8+j8 data inputs growing to a pair of 12+j12 outputs would require 80 pins alone, without microprogram control and coefficient inputs. As in the case of microprocessors, the solution to the pin limitation problem is the time-multiplexing of input/output data paths which could be tolerable for missile radar signal processing using buried-channel clocking rates. For higher performance avionic and air defense applications, multiple, two-chip CCD AU architectures (Figure 7.10) could be utilized without a significant hardware penalty.

7.6 Microcomputer Configurations

Of the four signal processor configurations reviewed, the CCD/CZT and CCD/FFT mechanizations appear to be the best candidates for low-chip-count monolithic VLSI packaging, thereby providing appropriate support circuit(s) for present VLSI microcomputers (Figure 7.11).

The CCD/CZT module is in effect a fixed-function, front-end processor, outputting the spectral components of radar returns for entry into microcomputer RAM via an A-D convertor and DMA I/O channel.

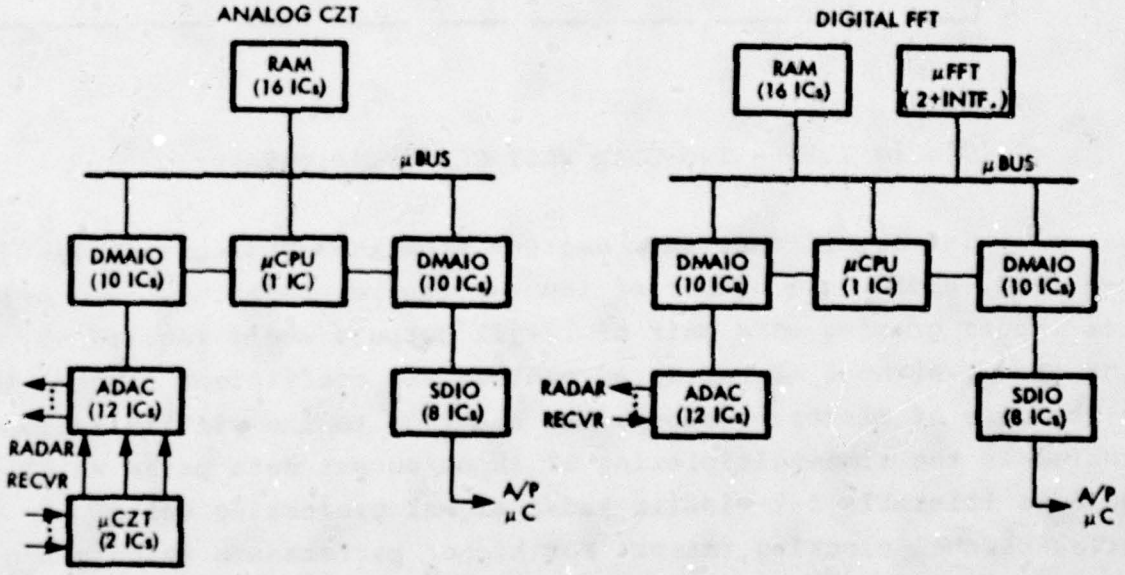


Figure 7.11 - CCD/CZT and CCD/FFT Microcomputer Configurations

By comparison, the CCD/FFT is an alternate mechanization of the original bipolar/CMOS-SOS μFFT module, connected to the μBus, with the potential of executing the PDI algorithm using the same butterfly AU.

7.7 Conclusions

Analog and digital CCD technology for military radar signal processing applications is still in the developmental stage. The need exists to reduce the physical size of existing high-performance real-time spectrum analyzers to fit into the new generation of imbedded microcomputer-based systems. Analog CCD/CZT and digital CCD/FFT mechanizations appear to have the potential for achieving two-chip monolithic VLSI with the necessary speed required for medium to high-performance radars. Digital CCD/FFT processors with microprogram control could conceivably execute alternate pipelineable, algorithms to further unburden the host microcomputer.

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APPENDIX A
MACROMODULAR MICROCOMPUTER SPECIFICATIONS

As a result of the additional device technology investigations performed during this phase of the study coupled with the earlier system analysis and module simulation work, a realistic set of seven microcomputer module specifications has been prepared.

The total number of individual module types has been reduced from fourteen (Section 3, Table 3.3) to eleven, based upon prototypes recently built; the advent of single chip commercial 16-bit microprocessors; and the elimination of the DMAIO module in favor of a more simple memory-mapped I/O scheme.

A listing of the seven module specifications covering the eleven module types is as follows:

1. Medium-Speed and High-Speed Microprocessors (μCPU-1 & μCPU-2)

2. Medium-Speed and High-Speed Read/Write and (Programmable) Read-Only Memories (RAM-1/(P)ROM-1 & RAM-2/(P)ROM-2)

3. High-Speed Frequency Spectrum Analyzer (FSA)

4. High-Speed Multiplier (HMPY)

5. Analog-to-Digital and Digital-to-Analog Convertor (ADAC)

6. Serial Digital Input-Output (SDIO)

7. Parallel Digital Input-Output (PDIO)

These specifications have been prepared in accordance with the requirements of military specification MIL-STD-490 for Critical Item Product Function Specifications Type C2a. Their purpose is to define only the performance interface, and acceptance requirements in order that multi-source, procurement of the modules can be exercised for a specific missile application. While the Navy SEM-1A and SEM-2A are the preferred plug-in module designs for each of the modules, specific missile form-factored modules are acceptable where space is limited, provided that the functional boundaries and μBus interface are maintained.

The chief objective of these specifications is, therefore, to control the functional boundaries and interface of microcomputer modules to achieve a variety of microcomputer configurations which cover the range of missile guidance and control system performance requirements. Further, the modules can be built using standard-industry microcomputer components and innovative cost-reduction design techniques, again, provided that the performance, interface and functional boundaries are maintained.

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
MEDIUM & HIGH SPEED
MICROPROCESSORS (μCPU-1 & μCPU-2)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the medium-speed and high-speed microprocessors, two very large-scale integrated-circuit (VLSIC) modules of the Navy Macromodular Microcomputer Family hereinafter referred to as μCPU-1 and μCPU-2 respectively, or the modules.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification

b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The medium-speed and high-speed microprocessor modules (μCPU-1 & μCPU-2) form two of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control applications.

Table 1 is a listing of the modules in the Family. Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities, in a federated microcomputer system for on-board missile guidance and control. From this data the need for both a medium and high speed microprocessor has been identified to cover the range of throughput requirements with minimum hardware. Both processors shall use the same support software and the same instruction repertoire.

3.1.1 Item Diagrams

The microcomputer modules which shall interface with the μCPUs via a standard microbus (μBus) are: read-write and (programmable) read-only memory (RAM/(P)ROM); analog-to-digital and digital-to-analog (ADAC) convertors; serial digital input-output (SDIO) module; parallel digital input-output module, (PDIO); high-speed frequency spectrum analyzer or fast Fourier transform module, (FSA) and a high-speed multiply module (HMPY), (Figure 2).

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

Module	Description	VSLI Circuit Technology	Application
µCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 600 nsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Control o Autopilot
µCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 150 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and µPCU Hybrids (2900/3000 Series or Equiv.) or Multi µCPU-1 Processor.	o Autopilot (Adaptive) o Signal Processing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement for µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 + J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/Write Memory, Medium Speed, 128-2Kx16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT

Module	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 µsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 µsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped. Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553A/B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

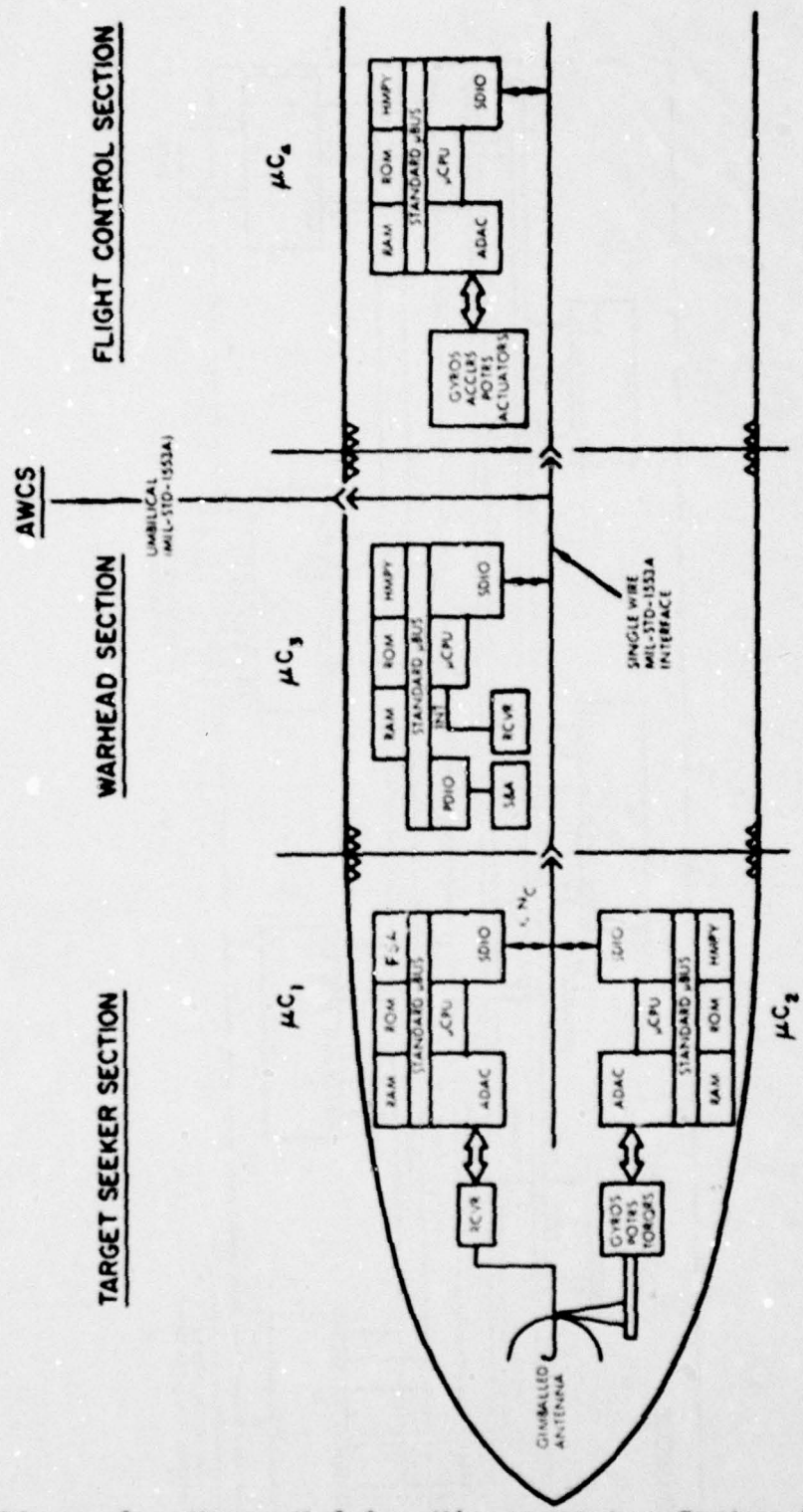

Figure 1 - Macro-Modular Microcomputer System for On-Board Missile Guidance and Control

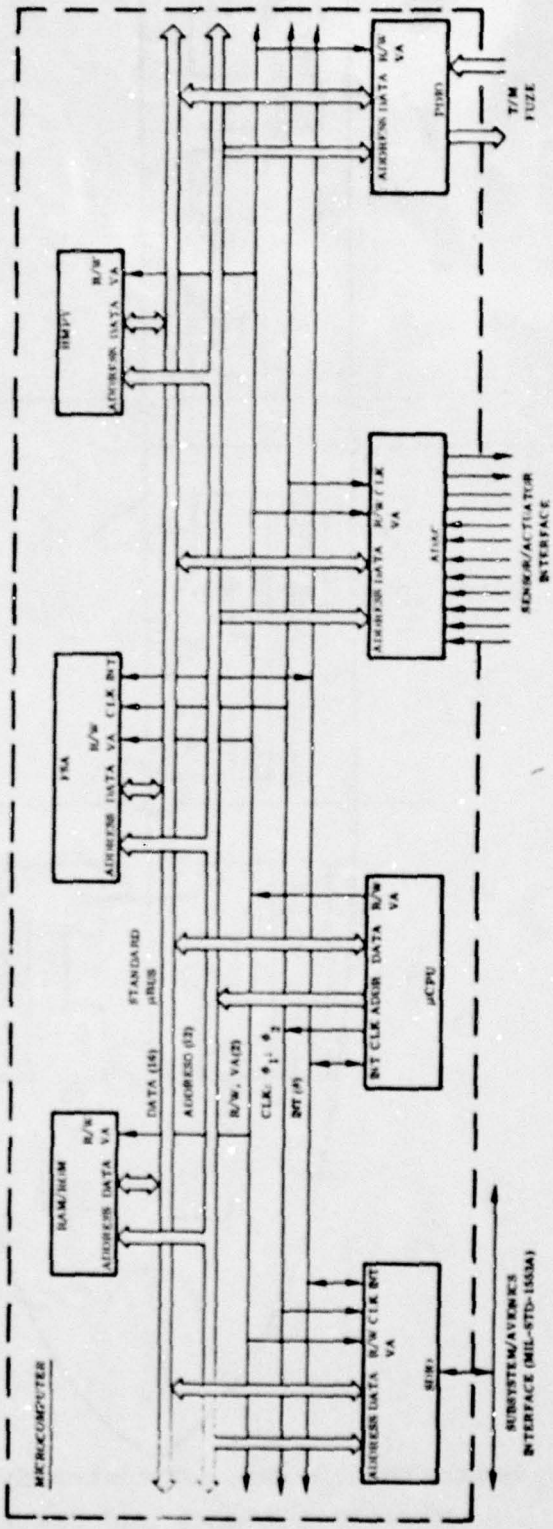

Figure 2 - Standard Microbus (μBus) Interface Lines

μCPU-1 and μCPU-2 shall interface with the microbus (μBus) of the microcomputer via tri-state drivers and receivers. Figure 2 shows the individual μBus interface lines and their use by the memory and input-output interface modules of the microcomputer.

A microbus interface module (MIM) shall be used to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface.

Figure 3 indicates the major functional elements of the μCPU-1 module and their interrelationship with one another. μCPU-2 shall be either a high-speed (CMOS-SOS) emulator of μCPU-1 or a multiprocessor using the same CPU-on-a-chip VLSI microprocessor as μCPU-1.

3.2 Characteristics

μCPU-1 and μCPU-2 shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for medium-speed and high-speed microprocessors in federated microcomputer systems. Only the significant architectural characteristics are specified to permit the choice of any suitable standard-industry microprocessor and combination of thereof to achieve the required performance.

3.2.1 Performance

μCPU-1 and μCPU-2 shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein. Whichever method is used to achieve the higher performance μCPU-2, (i.e.

bit-slice or multiprocessor architecture), μCPU-2 shall be programmable as a single processor, the same as μCPU-1.

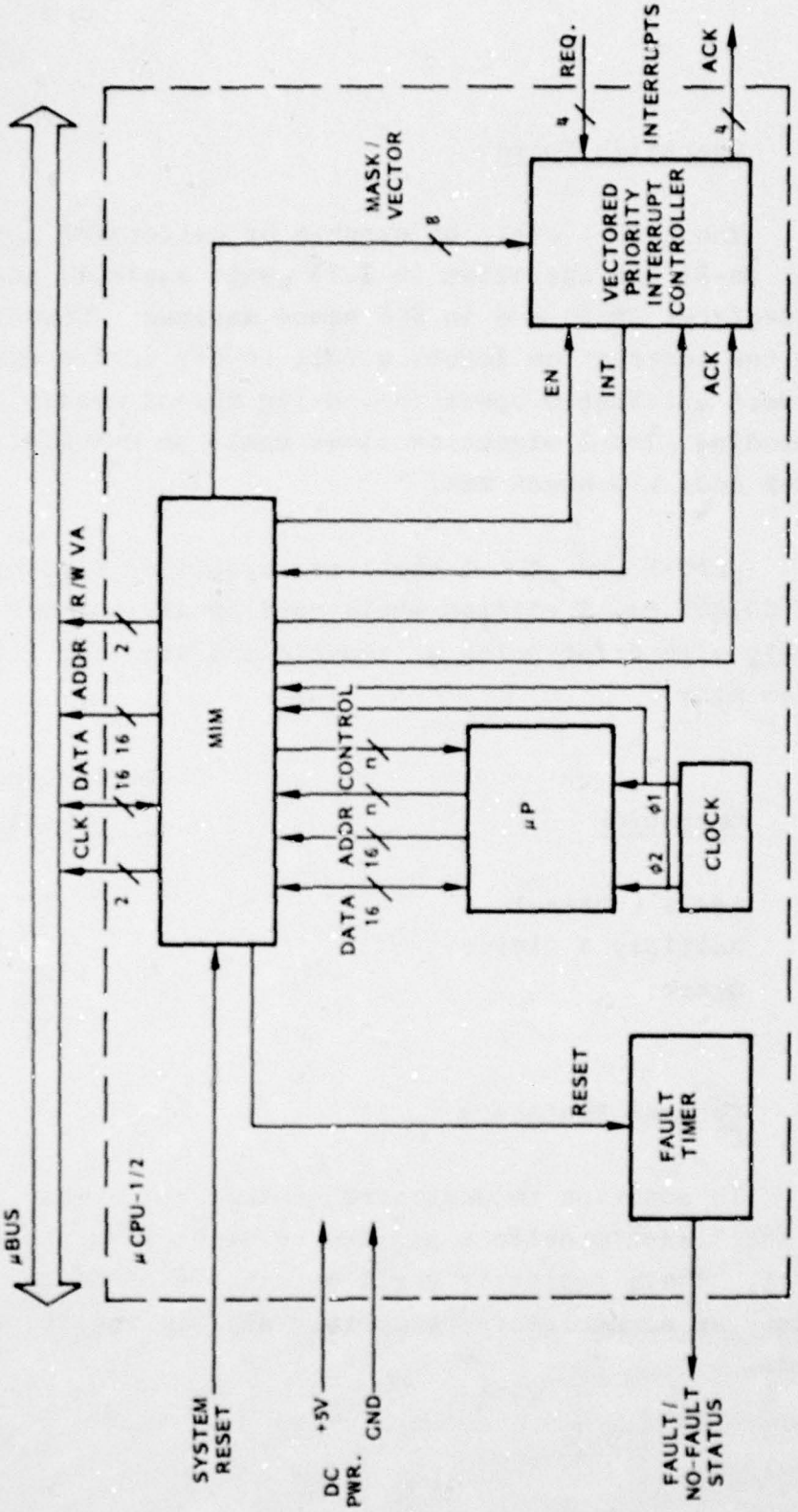

Figure 3 - General Block Diagram of μCPU-1/μCPU-2

3.2.1.1 Operation Speed

The μCPU-1 shall be capable of performing a memory-to-register (M-R) add operation in 2.75 μsecs maximum, and a register-to-register (R-R) add in 600 nsecs maximum. These times shall include the instruction fetch, a full 16-bit word operand fetch and a full word arithmetic operation, using direct memory addressing. Corresponding μCPU-2 execution times shall be M-R add: 600 nsecs max.; R-R add: 150 nsecs max.

μCPU-1 and μCPU-2 shall be capable of performing a minimum of 500,000 and 2 million whole word operations per second respectively with fixed-point arithmetic and with the following instruction mix:

Operation	Percentage of Total
Add & Subtract:	17
Multiply & Divide:	12
Other:	71
	100

3.2.1.2 General Registers

In addition to dedicated control registers, μCPU-1 and μCPU-2 shall each provide a minimum of eight 16-bit general-purpose registers. These registers shall be capable of being used by the programmer as accumulators, temporary storage registers and index registers.

3.2.1.3 Memory Addressing Modes

μCPU-1 and μCPU-2 shall provide the following four memory addressing modes as a minimum requirement.

a. Immediate - Operand contained in the current instruction word.

b. Direct/Absolute - Operand contained in a register or main memory location designated by an absolute address contained in the current instruction word.

c. Relative/Indexed - Operand located in main memory at the address obtained by adding/combining specific bits contained in the current instruction to the contents of a base/page register on the program counter.

d. Indirect - Operand located in main memory at an address contained in a register or main memory accessed by an address contained in the current instruction.

3.2.1.4 Internal Clock

An internal clock shall be provided in both μCPU-1 and μCPU-2 with sufficient output drive for the microprocessor and up to six other modules in a microcomputer configuration.

3.2.1.5 Fault Timer

μCPU-1 and μCPU-2 shall each contain a timer that must be reset by the microprocessor under program control at least once per second. If the timer is not reset at the prescribed time an external failure status line shall be enabled.

3.2.1.6 Program Interrupts

μCPU-1 and μCPU-2 shall provide a minimum of four program interrupts. Each interrupt shall cause the microprocessor to take its next instruction from a dedicated memory location associated with the interrupt.

Memory addresses that specify the dedicated location shall be permanently assigned. The interrupts if honored shall be taken upon completion of a current instruction. The program counter shall not be altered by the interrupt itself.

Each of the interrupts is individually maskable except as specified. Masked interrupts remain pending until unmasked and taken. The unmasking operation shall be structured such that the equipment is capable of handling multiple interrupts without the loss of return address linkages; i.e., an interrupt shall not be taken until the instruction following the unmasking instruction is executed.

The interrupt commands shall be capable of being configured in a priority structure. A higher priority interrupt shall not be inhibited while a lower priority interrupt is being honored. When an interrupt request is honored, it shall be automatically reset. The honored interrupt and all lower or equal priority inter-

rupts shall be automatically masked. They will remain masked until they are unmasked by an unmasking instruction and then a lower priority unmasked pending interrupt shall be honored.

3.2.1.7 Auto Reset

Upon applying power to μCPU-1 and μCPU-2 the contents of all registers shall be cleared to zero and the program counter shall commence incrementing through the program sequence.

3.2.2 Physical Characteristics

3.2.2.1 Overall Dimensions

The overall physical shape and dimensions of the module shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.2 Weight

The overall weight of the module shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The module shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The module shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The module shall meet the performance requirements of paragraph 3.2.1 during exposure to temperatures ranging from -28°C to +71°C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over the range specified in 3.2.5.1 at a rate of change of 1^{o} per second.

3.2.5.2 Shock

The module shall operate as specified herein after being subjected to $\pm$15 g peak shock impulse of 11 milliseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17 gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibrations associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure to a relative humidity of 95% at temperatures to +120°F.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be appropriately selected to meet the requirements of paragraph 3.2.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The module shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The module shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition, the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as applicable.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

TBDL

4.2 Quality Conformance Inspections

TBDL

5.0 PREPARATION FOR DELIVERY

TBDL

6.0 NOTES

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
MEDIUM & HIGH SPEED READ/WRITE AND
(PROGRAMMABLE) READ-ONLY MEMORIES
(RAM-1/(P)ROM-1 & RAM-2/(P)ROM-2)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER
FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the medium and high-speed Read/Write and (Programmable) Read-Only Memory modules of the Navy Macromodular Microcomputer Family hereinafter referred to as RAM-1/(P)ROM-1 and RAM-2/(P)ROM-2 respectively, or the modules.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification

b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The medium-speed and high-speed Read/Write and (Programmable) Read-Only Memory modules, RAM-1/(P)ROM-1 and RAM-2/(P)ROM-2 respectively, are four of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control applications.

Table 1 is a listing of the modules in the Family. Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities, in a federated microcomputer system for on-board missile guidance and control.

3.1.1 Item Diagrams

The microcomputer modules which shall interface with the RAMs/(P)ROMs via a standard microbus (μBus) are: microprocessors μCPU-1 and μCPU-2; analog to-digital and digital-to-analog (ADAC) convertors; serial digital input-output (SDIO) module; parallel digital input-output module, (PDIO); high-speed frequency spectrum analyzer or fast Fourier transform module, (FSA) and a high-speed multiply module (HMPY), Figure 2.

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

Module	Description	VSLI Circuit Technology	Application
µCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 2 µsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Control o Autopilot
µCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 400 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and µPCU Hybrids (2900/3000 Series or Equiv.) or Multi µCPU-1 Processor.	o Autopilot (Adaptive) o Signal Processing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement for µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 + J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/ Write Memory, Medium Speed, 128-2K×16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/ Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits or 256-2K Bytes, 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits or 1K-8K Bytes 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT

Module	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 µsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 µsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553A/B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

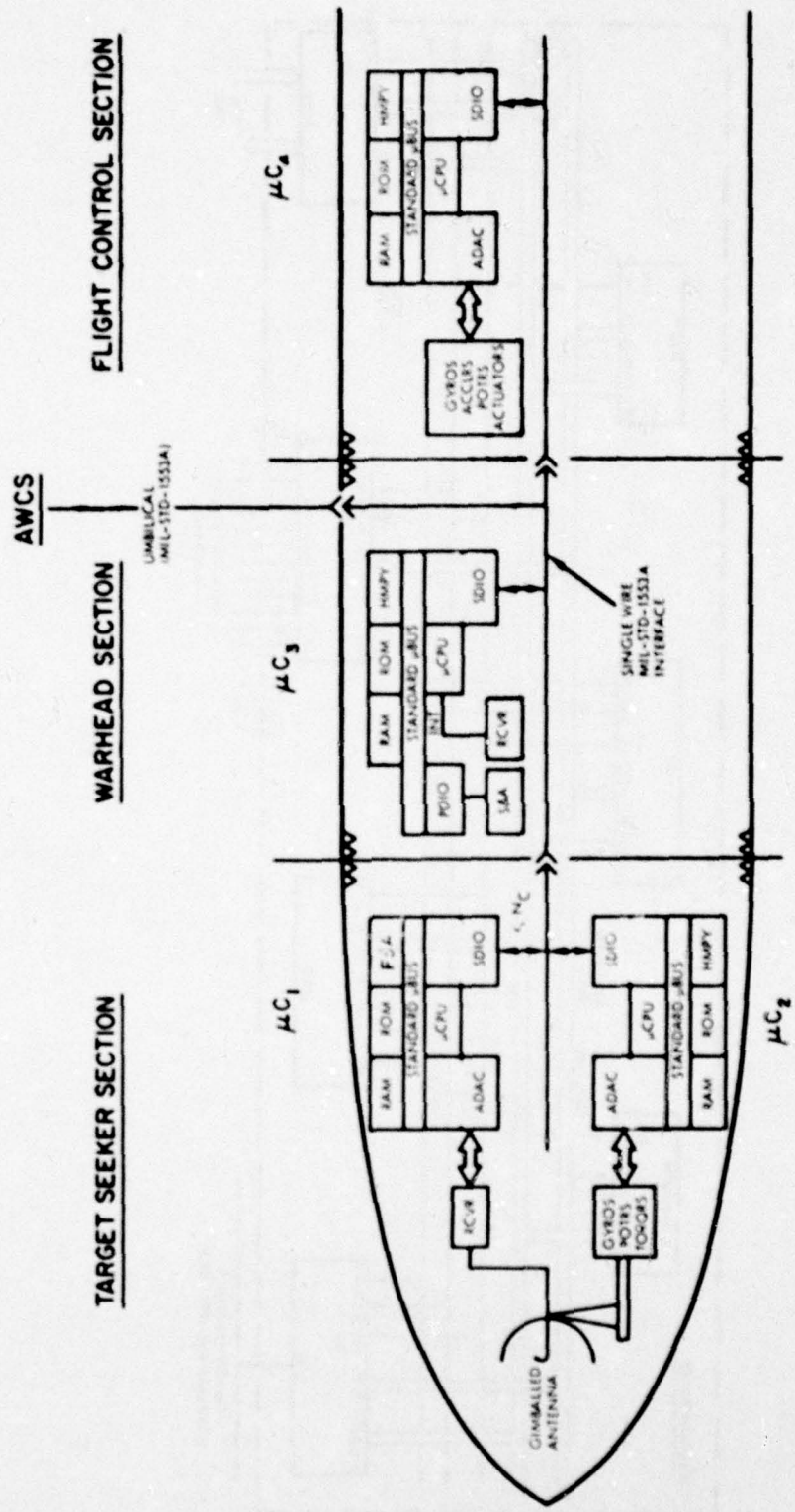

Figure 1 - Macro-Modular Microcomputer System for On-Board Missile Guidance and Control

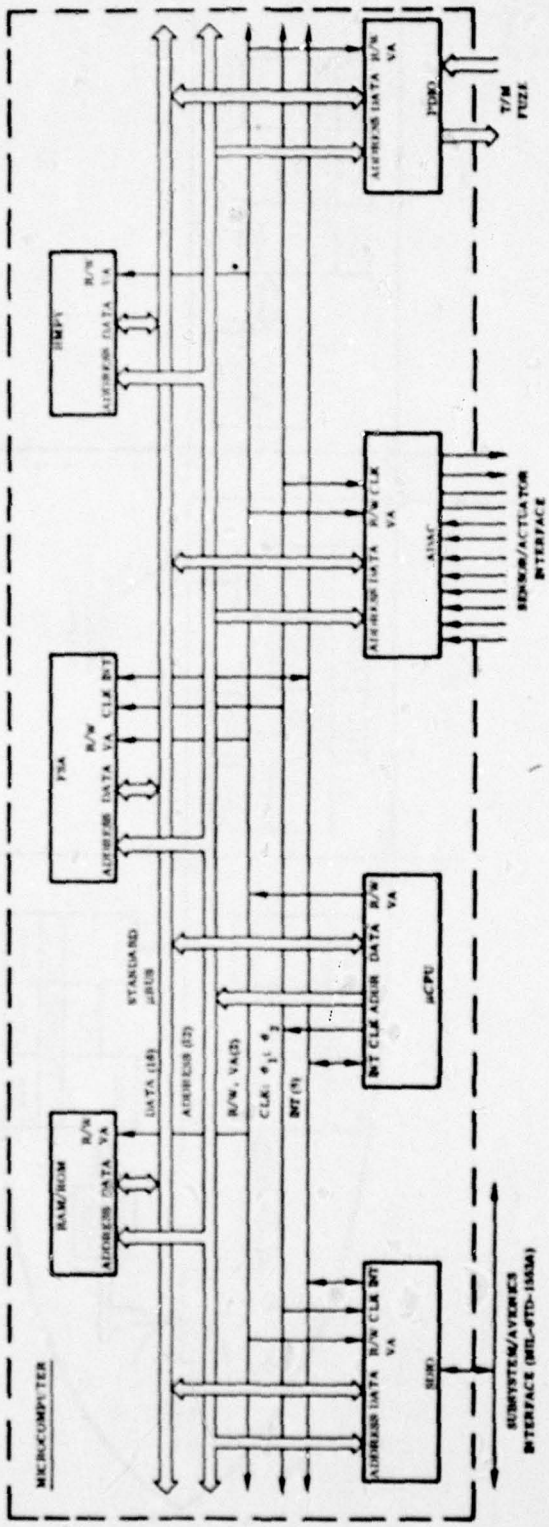

Figure 2 - Standard Microbus (μBus) Interface Lines

RAM and ROM, or alternatively programmable read-only memory, (PROM), modules shall interface with the microbus (μBus) via tri-state drivers and receivers and provide programmable chip and word decoding for flexible memory mapping. Two speeds of memory shall be provided. RAM-1 and (P)ROM-1 shall be high-density medium-speed memories and RAM-2 and (P)ROM-2 shall be high-speed memories, (see performance requirements).

A microbus interface module (MIM) shall be used to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface, and to provide programmable memory mapping of RAMs and (P)ROMs.

Figure 3 indicates the major functional elements of the RAMs/(P)ROMs and their interrelationship with one another.

3.2 Characteristics

RAMs/(P)ROMs shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for the RAM/(P)ROM modules in federated microcomputer systems. Only the significant characteristics are specified to permit the choice of any suitable standard-industry components and combination of thereof to achieve the required performance.

3.2.1 Performance

RAM/(P)ROM modules shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein.

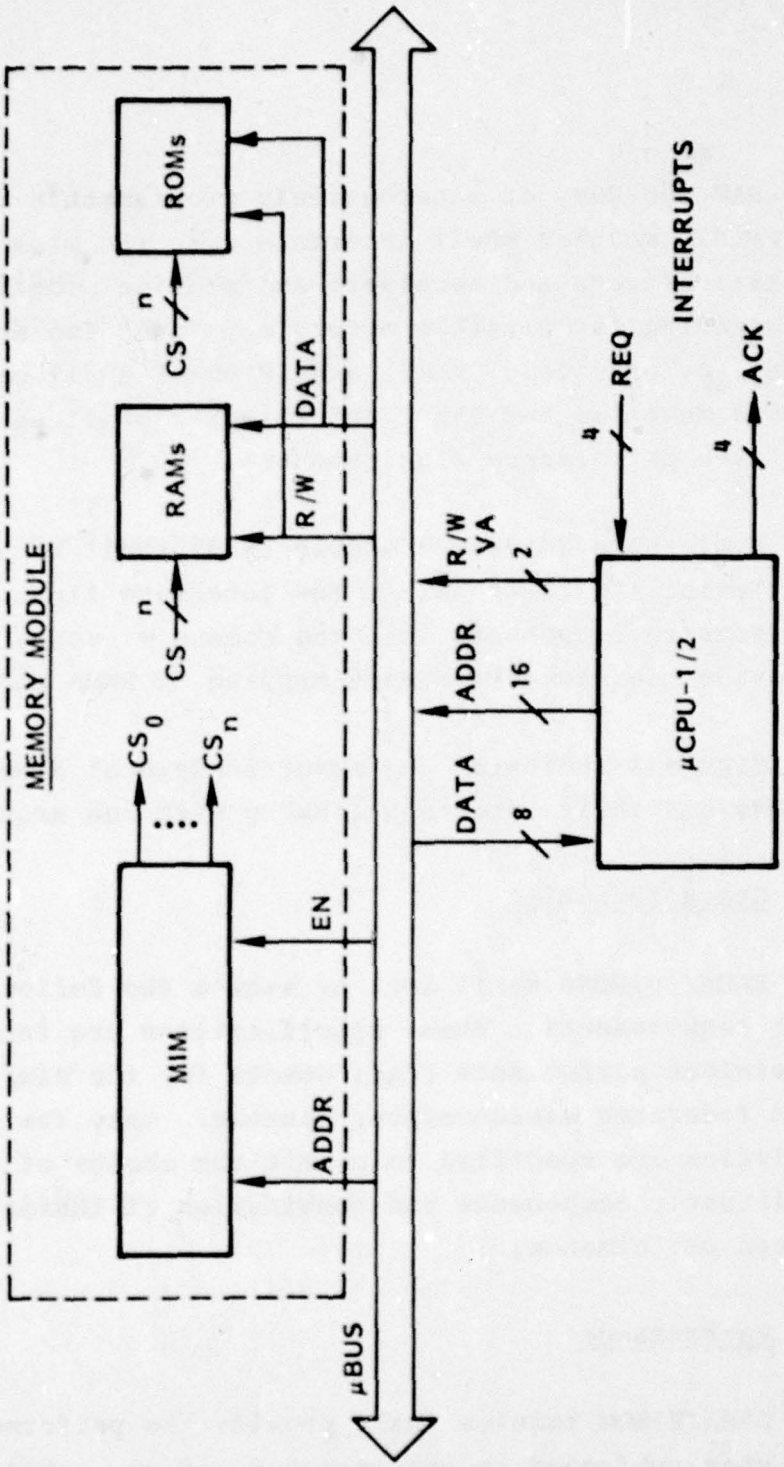

Figure 3 - General Block Diagram of the RAM/(P)ROM Modules

RAM-1	Access Time (nsecs):	500 max.
	Capacity (words) :	2048 max.
(P)ROM-1	Access Time (nsecs):	500 max.
	Capacity (words) :	16384 max.
RAM-2	Access Time (nsecs):	100 max.
	Capacity (words) :	1024 max.
(P)ROM-2	Access Time (nsecs):	100 max.
	Capacity (words) :	4096 max

3.2.2 Physical Characteristics

3.2.1.1 Overall Dimensions

The overall physical shape and dimensions of the modules shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module.

3.2.2.2 Weight

The overall weight of the modules shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The modules shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The modules shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The modules shall meet the performance requirements of paragraph 3.2.1 during exposure to temperature ranging from -28°C to +71°C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over that range specified in 3.2.5.1 at a rate of change of 1^{o} per second.

3.2.5.2 Shock

The module shall operate as specified herein after being subjected to ±15g peak shock impulse of 11 milliseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibration associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure to a relative humidity of 95% at temperatures to $+120^{o}F$.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be selected to meet the requirements of paragraph 3.2.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The modules shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The modules shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition,

the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as appropriate.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

TBDL

4.2 Quality Conformance Inspections

TBDL

5.0 PREPARATION FOR DELIVERY

6.0 NOTES

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
HIGH SPEED
FREQUENCY SPECTRUM ANALYZER
(FSA)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the High-Speed Frequency Spectrum Analyzer (FSA) module of the Navy Macromodular Microcomputer Family hereinafter referred to as the module.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification

b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The High-Speed Frequency Spectrum Analyzer (FSA) module is one of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control applications.

Table 1 is a listing of the modules in the Family. Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities in a federated microcomputer system for on-board missile guidance and control.

The FSA module shall provide a high-speed fast Fourier transform (FFT) or equivalent capability where a software implementation of the algorithm is too slow for certain missile signal processing applications. Access to the FSA shall be via the μBus, in the same manner as the other modules in the Family, Figure 2.

3.1.1 Item Diagrams

Figure 3 shows the main functional components of the FSA and their interrelationship with one another. Two RAMs shall form the interface between the arithmetic and control circuits of the FSA and the MIM. Complete data samples shall be loaded into these RAMs by the microprocessor in any desired order for rapid processing by the FSA.

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

MODULE	Description	VSLI Circuit Technology	Application
µCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 600 nsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Control o Autopilot
µCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 150 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and µPCU Hybrids (2900/3000 Series or Equiv.) or Multi µCPU-1 Processor.	o Autopilot (Adaptive) o Signal Processing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

MODULE	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement for µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 ÷ J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/Write Memory, Medium Speed, 128-2Kx16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

MODULE	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT

MODULE	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 μsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 μsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped. Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553A/B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

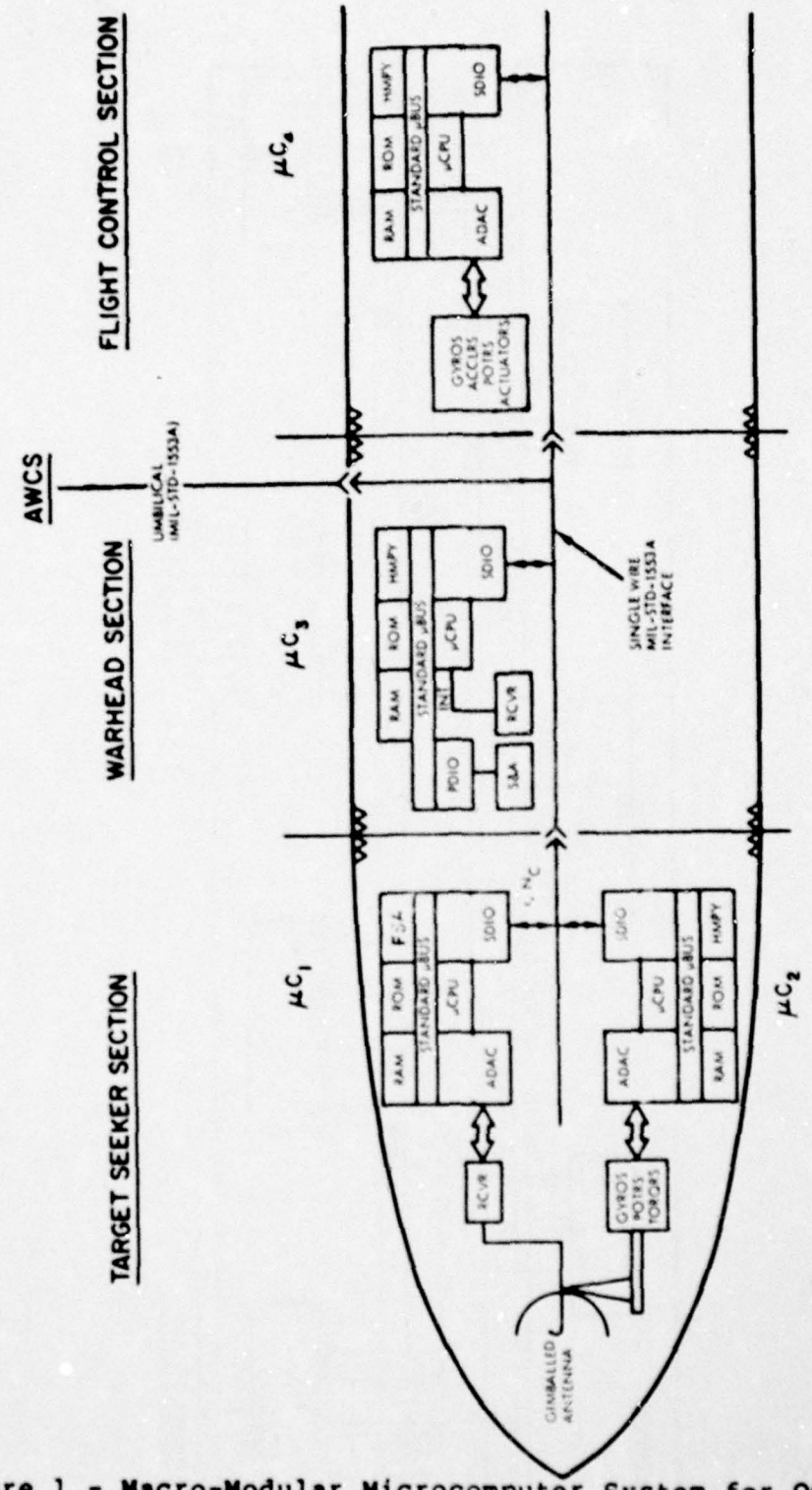

Figure 1 - Macro-Modular Microcomputer System for On-Board Missile Guidance and Control

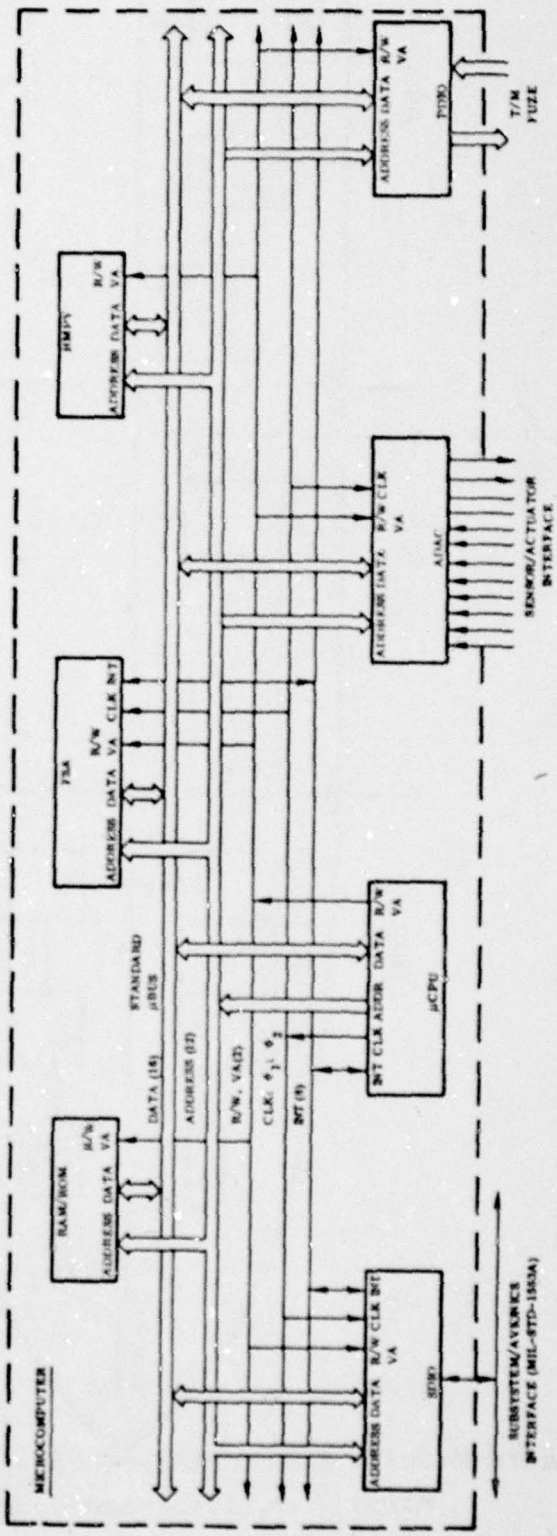

Figure 2 - Standard Microbus (μBus) Interface Lines

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MODULAR DIGITAL MISSILE GUIDANCE.(U)
DEC 79 F J LANGLEY , A J MANNION , K D LAUBE N00014-75-C-0549
UNCLASSIFIED BR-11344 ONR-CR233-052-4 NL

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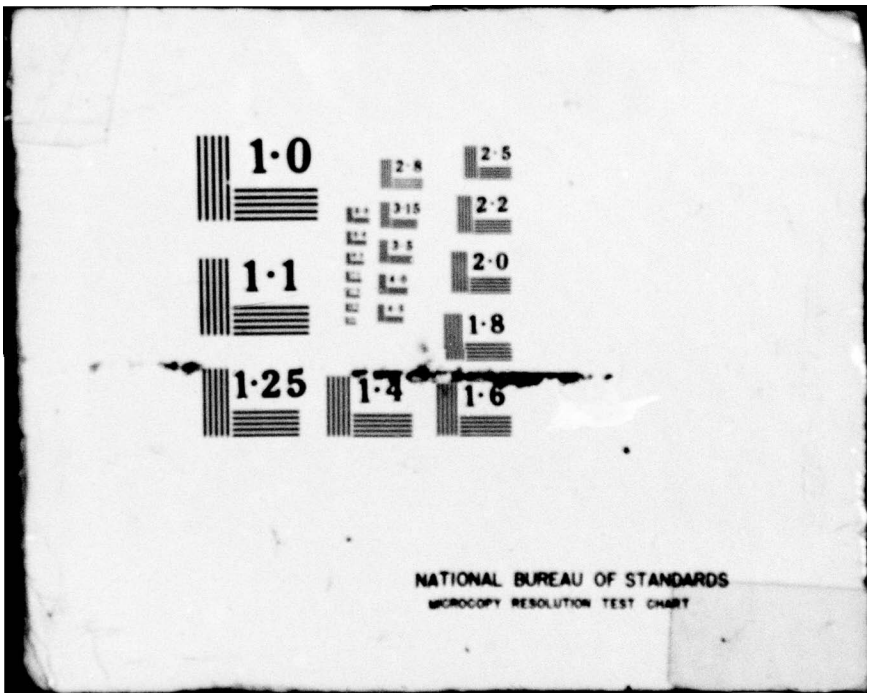
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NATIONAL BUREAU OF STANDARDS
MICROCOPY RESOLUTION TEST CHART

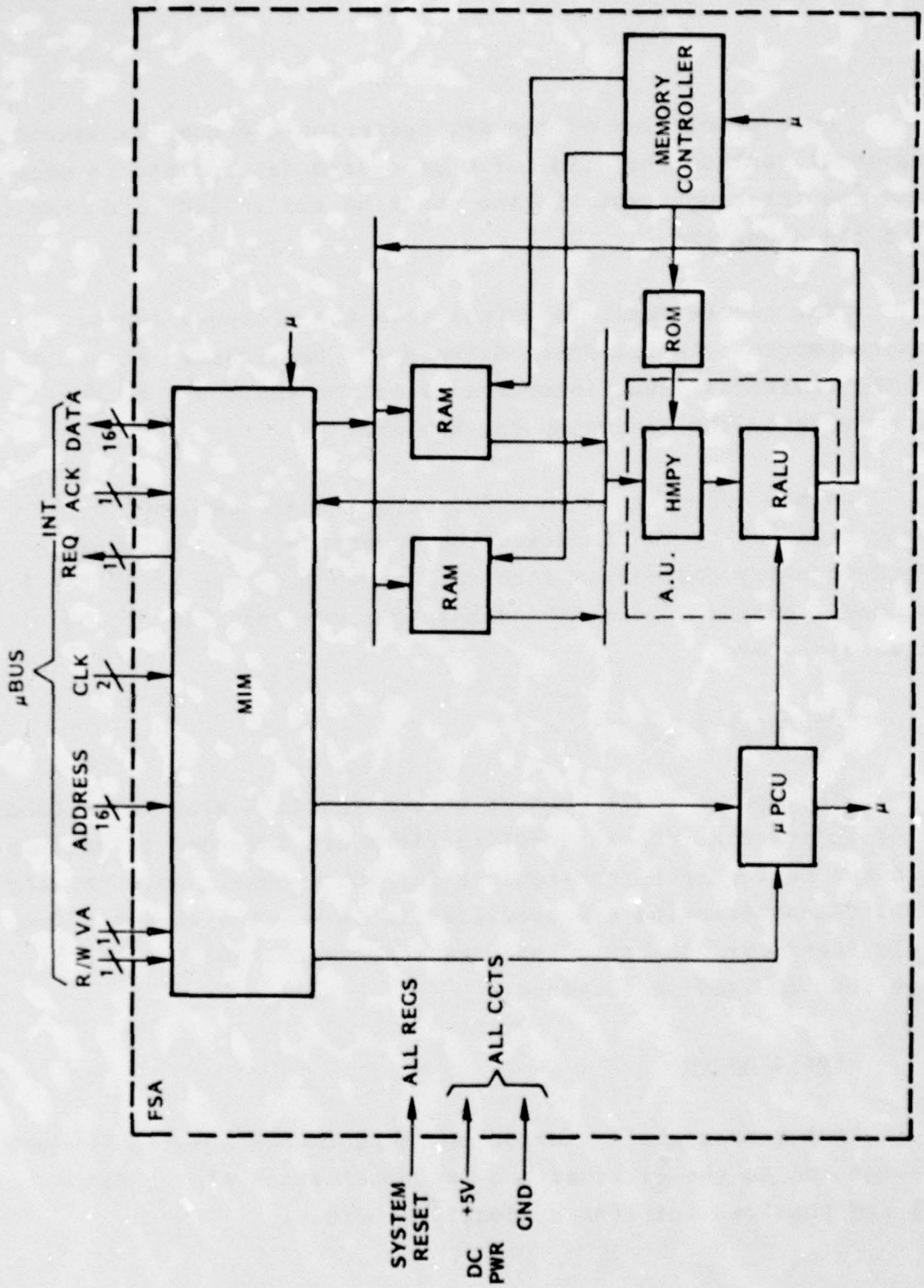

Figure 3 - General Block Diagram of the FSA Module

Upon completion of the FFT operation the complex spectral values shall replace the original unprocessed data points in each RAM and the interrupt request-line shall be set to indicate completion of the algorithm.

The module shall interface with the microbus (μBus) of the microcomputer via tri-state drivers and receivers. Figure 2 shows the individual μBus interface lines and their use by the other modules of the microcomputer family.

A microbus interface module (MIM) shall be used to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface and to map the location of the RAMs within any desired area of the total memory space.

3.2 Characteristics

The module shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for the module. Only the significant characteristics are specified to permit the choice of any suitable standard-industry components and combination thereof to achieve the required performance.

3.2.1 Performance

The module shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein.

No. of complex points:	64, 128 and 256, (preset, by external pin linkage).
Magnitude:	8 + j8, input 12 + j12, output
FFT execution time: (μsecs. max.)	150, 350, 800, for 64, 128 and 256 cplx, points respectively.

3.2.2 Physical Characteristics

3.2.2.1 Overall Dimensions

The overall physical shape and dimensions of the module shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.2 Weight

The overall weight of the module shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The module shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The module shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The module shall meet the performance requirements of paragraph 3.2.1 during exposure to temperature ranging from -28°C to +71°C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over the range specified in 3.2.5.1 at a rate of change of 1^{o} per second.

3.2.5.2 Shock

The module shall operate as specified herein after being subjected to ±15g peak shock impulse of 11 milliseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibration associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure to a relative humidity of 95% at temperatures to $+120^{o}F$.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be appropriately selected to meet the requirements of paragraph 3.2.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The module shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The module shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition,

the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as applicable.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

TBDL

4.2 Quality Conformance Inspections

TBDL

5.0 PREPARATION FOR DELIVERY

TBDL

6.0 NOTES

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
HIGH SPEED
MULTIPLY MODULE (HMPY)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the High Speed Multiply Module (HMPY) module of the Navy Macromodular Microcomputer Family hereinafter referred to as the module.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification

b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The High Speed Multiply Module (HMPY) forms one of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control appli-cations.

Table 1 is a listing of the modules in the Family. Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities, in a federated microcomputer system for on-board missile guidance and control.

3.1.1 Item Diagrams

The microcomputer modules which shall interface with the HMPY via a standard microbus (μBus) are: microprocessors μCPU-1 and μCPU-2 read-write and (programmable) read-only memory (RAM/(P)ROM); analog-to-digital and digital-to-analog (ADAC) convertors; serial digital input-output (SDIO) module; parallel digital input-output module, (PDIO); and a high-speed frequency spectrum analyzer or fast Fourier transform module, (FSA), (Figure 2).

HMPY shall interface with the microbus (μBus) of the microcomputer via tri-state drivers and receivers. Figure 2 shows the individual μBus interface lines and their use by the memory and input-output interface modules of the microcomputer.

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

Module	Description	VSLI Circuit Technology	Application
µCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 600 nsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Control o Autopilot
µCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 150 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and µPCU Hybrids (2900/3000 Series or Equiv.) or Multi µCPU-1 Processor.	o Autopilot (Adaptive) o Signal Processing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement for µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 + J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/Write Memory, Medium Speed, 128-2Kx16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT

Module	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 µsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 µsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped. Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553A/B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

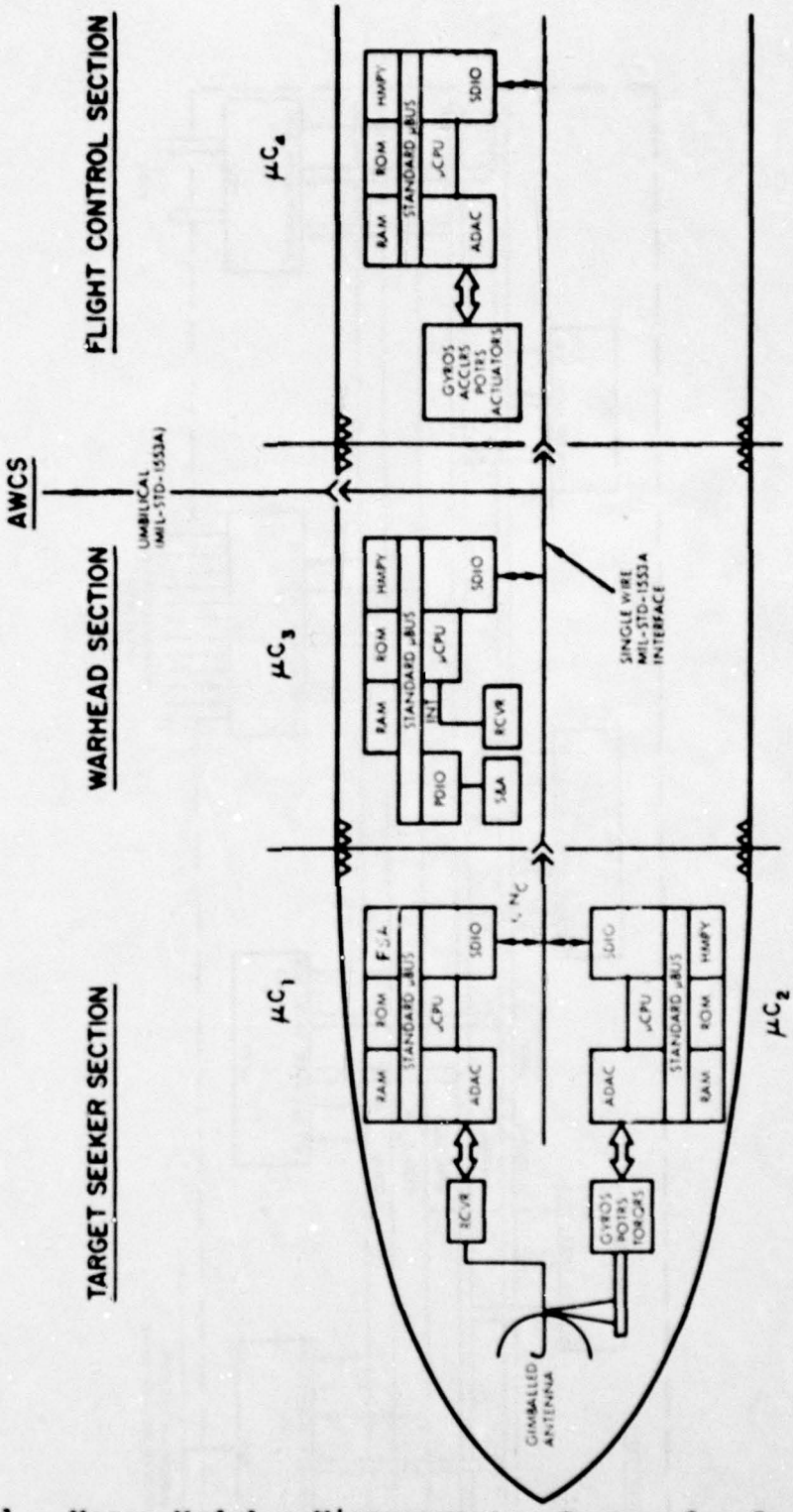

Figure 1 - Macro-Modular Microcomputer System for On-Board Missile Guidance and Control

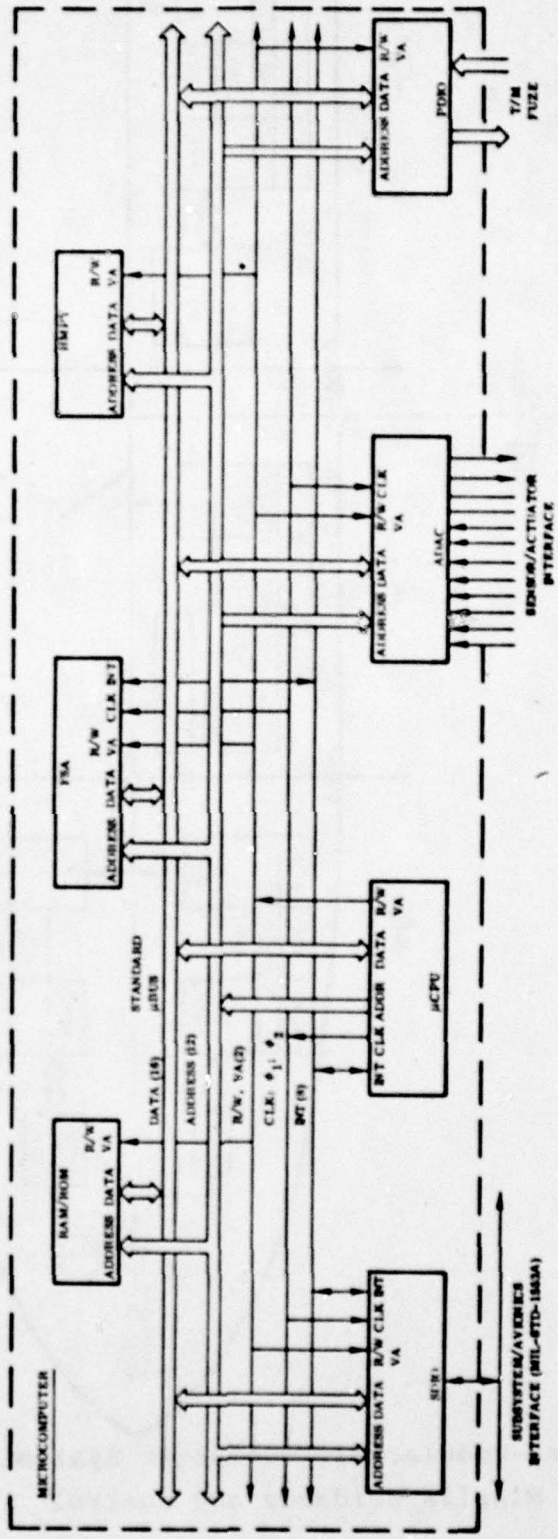

Figure 2 - Standard Microbus (μBus) Interface Lines

A microbus interface module (MIM) shall be used to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface.

The HMPY module shall provide storage for a 16-bit multiplier, 16-bit multiplicand and the 16 most significant bits of their product. All the latter data words shall be in 2's complement form. The storage of all data words shall be addressable as part of the total memory map of the microcomputer. The location of these words in the total memory map shall be programmable within the MIM.

Figure 3 indicates the major functional elements of the HMPY module and their interrelationship with one another.

3.2 Characteristics

HMPY shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for the HMPY module. Only the significant characteristics are specified to permit the choice of any suitable standard-industry components and combination thereof to achieve the required performance.

3.2.1 Performance

The HMPY module shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein.

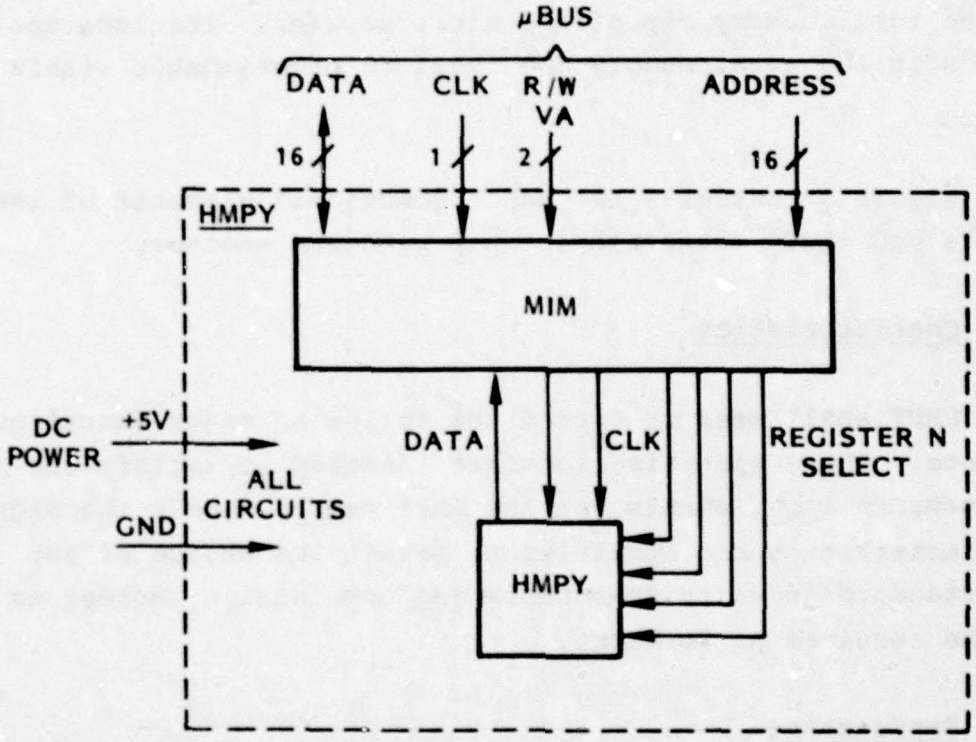

Figure 3 - General Block Diagram of High Speed Multiply Module

3.2.1.1 Execution/Cycle Time

The HMPY module shall perform a 16-bit x 16-bit multiply in 100 nsecs, max.

3.2.1.2 Storage

Capacity: 3 x 16 Bits (Multiplier, Multiplicand, and 16 MSB of Product).

3.2.2 Physical Characteristics

3.2.2.1 Overall Dimensions

The overall physical shape and dimensions of the module shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.2 Weight

The overall weight of the module shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The module shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The module shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The module shall meet the performance requirements of paragraph 3.2.1 during exposure to temperatures ranging from -28°C to +71° C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over the range specified in 3.2.5.1 at a rate of change of 1^{o} per second.

3.2.5.1 Shock

The module shall operate as specified herein after being subjected to ±15 g peak shock impulse of 11 milliseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17 gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibrations associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure to a relative humidity of 95% at temperatures to $+120^{o}F$.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be appropriately selected to meet the requirements of paragraph 3.2.1.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The module shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The module shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition, the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as applicable.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

TBDL

4.2 Quality Conformance Inspections

TBDL

5.0 PREPARATION FOR DELIVERY

TBDL

6.0 NOTES

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
ANALOG TO DIGITAL/DIGITAL TO
ANALOG CONVERTOR (ADAC)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the Analog to Digital/Digital to Analog convertor (ADAC) module of the Navy Macromodular Microcomputer Family hereinafter referred to as the ADAC or the module.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification

b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The Analog to Digital and Digital to Analog Convertor (ADAC) forms one of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control applications.

Table 1 is a listing of the modules in the Family and Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities for on-board missile guidance and control. The ADAC module shall provide the interface between a microcomputer and various missile analog sensors and actuators.

3.1.1 Item Diagrams

Figure 2 shows the ADAC module as part of several complete microcomputer configurations. The microcomputer modules which shall interface with the ADAC via a standard microbus (μBus) are: medium and high-speed μCPU-1 and μCPU-2 modules; read-write and (programmable) read-only memory (RAM/(P)ROM); serial digital input-output (SDIO) module; parallel digital input-output module, (PDIO); high-speed frequency spectrum analyzer or fast Fourier transform module, (FSA) and a high-speed multiply module (HMPY).

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS			
Module	Description	VSLI Circuit Technology	Application
μCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 600 nsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Control o Autopilot
μCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 150 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and μPCU Hybrids (2900/3000 Series or Equiv.) or Multi μCPU-1 Processor.	o Autopilot (Adaptive) o Signal Processing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement for µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 + J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/Write Memory, Medium Speed, 128-2Kx16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT			
Module	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 μsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 μsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped. Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

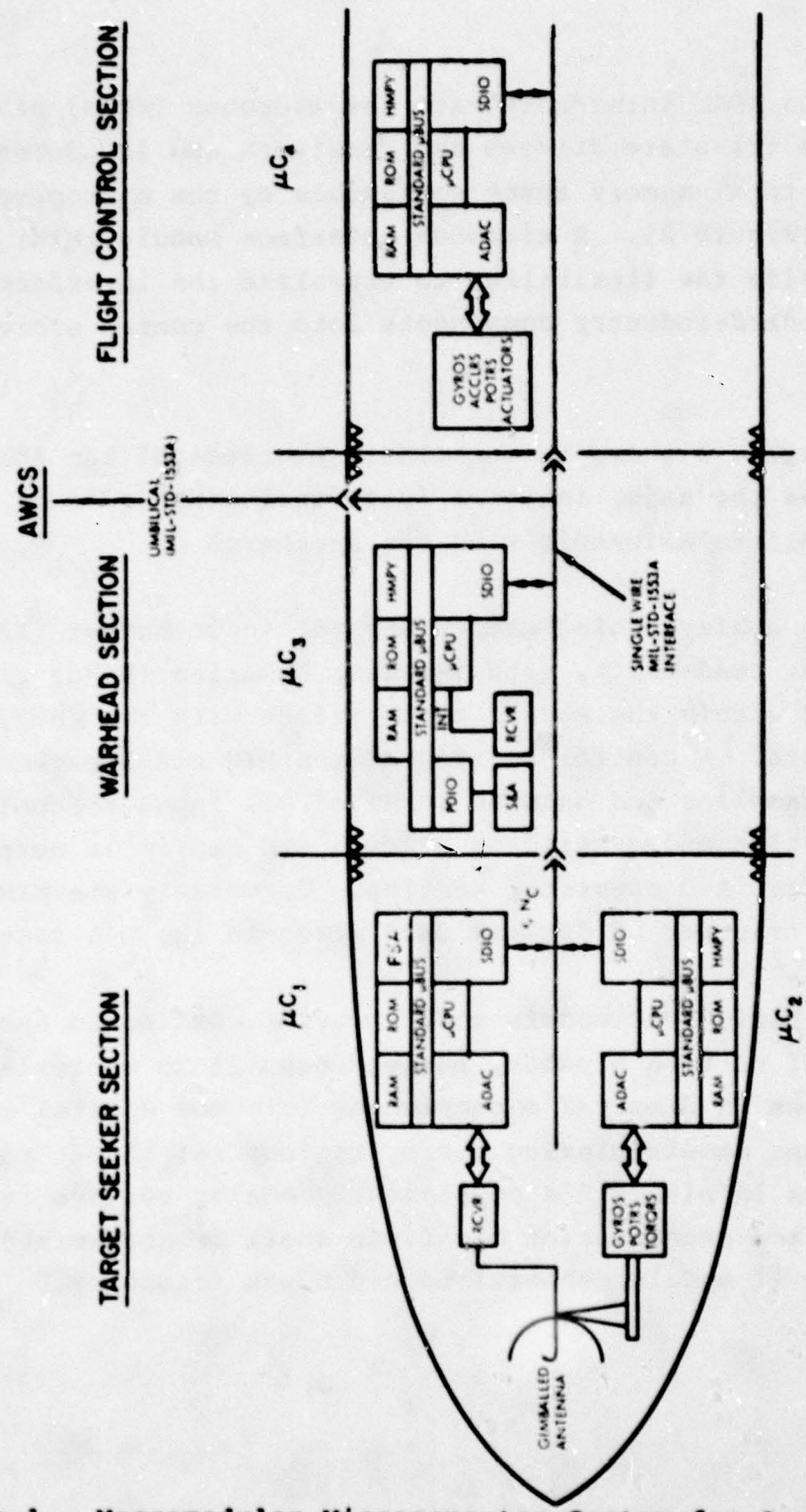

Figure 1 - Macromodular Microcomputer System for On-Board Missile Guidance and Control

The ADAC interfaces with the microbus (μBus) of the microcomputer via tri-state drivers and receivers and is addressed as part of the total memory space accessible by the microprocessor module (μCPU) (Figure 2). A microbus interface module (MIM) shall be used to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface.

Figure 3 shows the external interface of the ADAC module and indicates the major internal functional components of the ADAC and their interrelationship with one another.

To achieve this "memory-mapped" input-output (I/O) mode of operation, read-write, random-access memories (RAMs) are incorporated within the module to interface with the μBus, A-D and D-A convertors. A control section of the MIM shall perform the simultaneous sampling and holding (S/H) of all input channels and the cyclic selection and quantizing of each S/H amplifier output via the multiplexer A-D convertor section. Conversely the MIM shall control the transfer of digital data words to the D-A convertors.

A basic ADAC module shall provide continuous sampling and conversion of up to 8 bipolar, analog channels to equivalent 12-bit digital values in binary 2's complement form and digital to analog conversion and demultiplexing for up to four (4) 12 bit parallel digital words in binary 2's complement. Analog voltage ranges, sampling rates and quantization magnitude shall be determined by external patching of module connections and clock frequency.

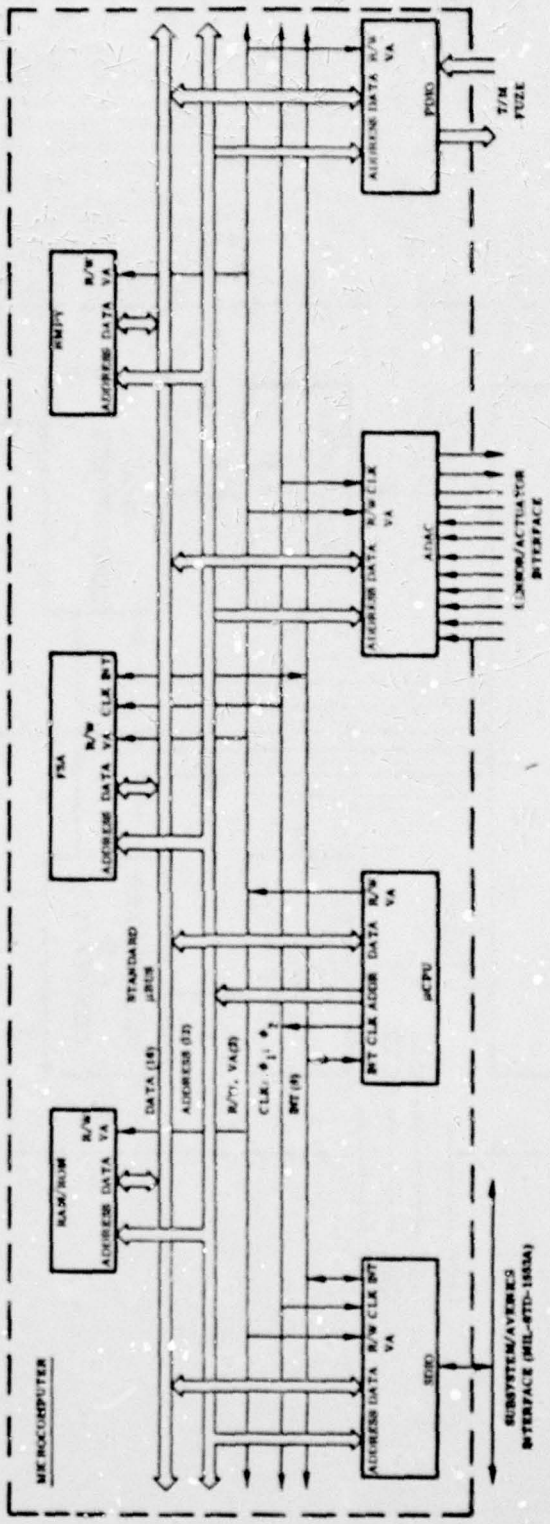

Figure 2 - Standard Microbus (μBus) Interface Lines

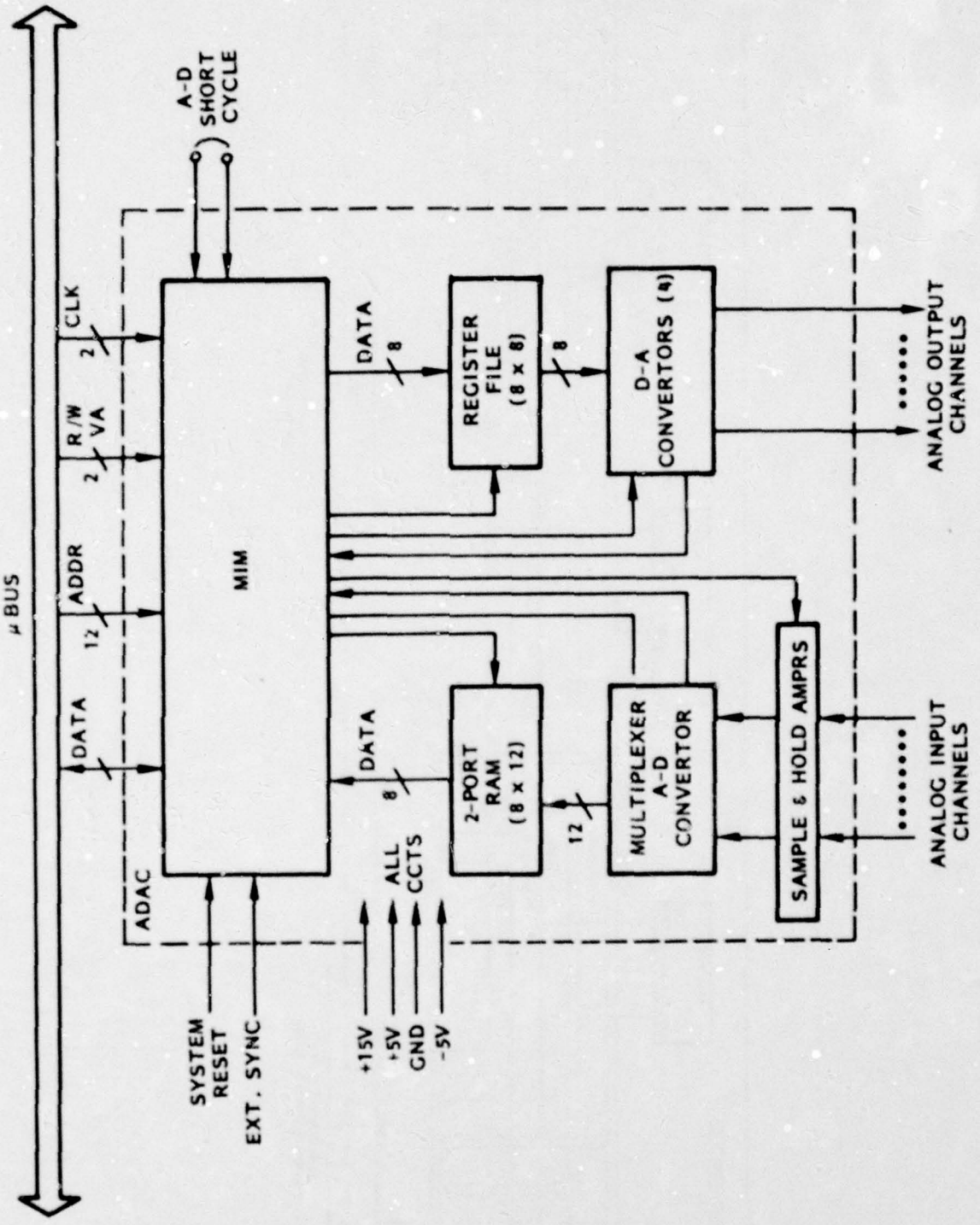

Figure 3 - ADAC Functional Block Diagram

3.2 Characteristics

The ADAC module shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for the ADAC. Only the significant characteristics are specified to permit the choice of any suitable standard-industry components and combination of thereof to achieve the required performance.

3.2.1 Performance

The ADAC module shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein.

3.2.1.1 Multiplexer A-D Converter

Resolution:	12 bits; 8 bits short cycle
No. of Channels:	8 (16 single-ended/8 differentials) expandable in increments of 8, up to 24 chs.
Analog Input Voltage Ranges:	0 to ±5V, ±5V and ±10V, preset by external pin connections.
Throughput:	8/3 μsec max.perch for 12 or 8-bit quantizing respectively.
Accuracy:	±0.024% Full-Scale Range (FSR)
Linearity:	±0.012% FSR
Aperture Time:	100 nsec
Digital Output Code:	Binary, 2's Complement.

3.2.1.2 D-A Convertors

Digital Input:	12 bits, binary 2's Cplt.
Linearity Error:	±½ LSB
Gain Error:	±0.1% FSR adjustable
Offset Error:	±0.05% FSR to zero
Settling Time	1.5 max. (1 LSB change)
to ± 0.1% FSR	0.3 max. (F/S change)
(μsecs):	
Analog Output	
(Volts):	±10, ±5, ±2.5, 0 to +10 or 0 to 5, (externally patched).
Analog D.C. Output	
Impedance (ohms):	0.05 max.
Analog Output	±5mA min.
(Current):	

3.2.2 Physical Characteristics

3.2.2.1 Overall Dimensions

The overall physical shape and dimensions of the module shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.2 Weight

The overall weight of the module shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The module shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The module shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The module shall meet the performance requirements of paragraph 3.2.1 during exposure to temperature ranging from -28°C to +71°C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over the range specified in 3.2.5.1 at a rate of change of 1° per second.

3.2.5.2 Shock

The module shall operate as specified herein after being subjected to ±15g peak shock impulse of 11 milliseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibration associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure to a relative humidity of 95% at temperatures to +120°F.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be appropriately selected to meet the requirements of paragraph 3.2.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The module shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The module shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition, the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as applicable.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

TBDL

4.2 Quality Conformance Inspections

TBDL

5.0 PREPARATION FOR DELIVERY

TBDL

6.0 NOTES

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
SERIAL DIGITAL
INPUT OUTPUT
(SDIO)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the Serial Digital Input Output (SDIO) module of the Navy Macromodular Microcomputer Family hereinafter referred to as the module.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-1553	Military Standard Aircraft Internal Time Division Command/Response Multiplex Data Bus

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification
b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The Serial Digital Input Output module forms one of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control applications.

Table 1 is a listing of the modules in the Family. Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities in a federated microcomputer system for on-board missile guidance and control.

The SDIO module performs the conversion of 16-bit parallel data words into a serial digital bit stream and vice versa. The parallel digital interface shall comply with the μBus interface requirements and the serial digital input - output shall comply with the requirements of military standard specification MIL-STD-1553B, herein after referred to as 1553B. However, the use of a fiber-optic communication link between SDIO modules shall be acceptable, provided that the integrity of the link complies with the performance requirements of 1553B.

Interface with the μBus shall be via a programmable microbus interface module (MIM). Two RAMs, for input and output data storage respectively, shall form part of the microcomputer memory-mapped I/O scheme.

Each SDIO module shall be capable of operating as a master or a slave on the 1553B multiplexed bus system. Sensing of either mode of operation shall be determined from control words placed in the transmit RAM under microprocessor program control.

The SDIO shall receive 16-bit data words via the μBus and translate them into appropriate message formats complying with the requirements of MIL-STD-1553B.

The communication protocol required to establish a link and to transfer data between two SDIO modules shall be performed internally by the SDIO, i.e. within the MIM.

Conversely, when not transmitting 1553B messages, the SDIO shall monitor the bus continuously and, upon recognition of an address code correlating with a pre-programmed unique device address code stored in the SDIO, the SDIO shall extract the 16-bit data words from the incoming serial digital messages and store these data in the "receive" RAM. Only valid data, i.e. data satisfying parity checks, shall be stored in the RAM for access by the microprocessor module (μCPU-1/2).

3.1.1 Item Diagrams

The microcomputer modules which shall interface with the SDIO via a standard microbus (μBus) are: microprocessors μCPU-1 and μCPU-2; read-write and (programmable) read-only memory (RAM/(P)ROM; analog-to-digital and digital-to-analog (ADAC) convertors; parallel digital input-output module, (PDIO); high-speed frequency spectrum analyzer or fast Fourier transform module, (FSA) and a high-speed multiply module (HMPY), Figure 2.

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

Module	Description	VSLI Circuit Technology	Application
μCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 600 nsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Con- o Autopilot
μCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 150 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and μPCU Hybrids (2900/3000 Series or Equiv.) or Multi μCPU-1 Processor.	o Autopilot (Adaptive) o Signal Pro cessing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 + J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/Write Memory, Medium Speed, 128-2Kx16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT

Module	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 μsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 μsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped. Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553A/B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

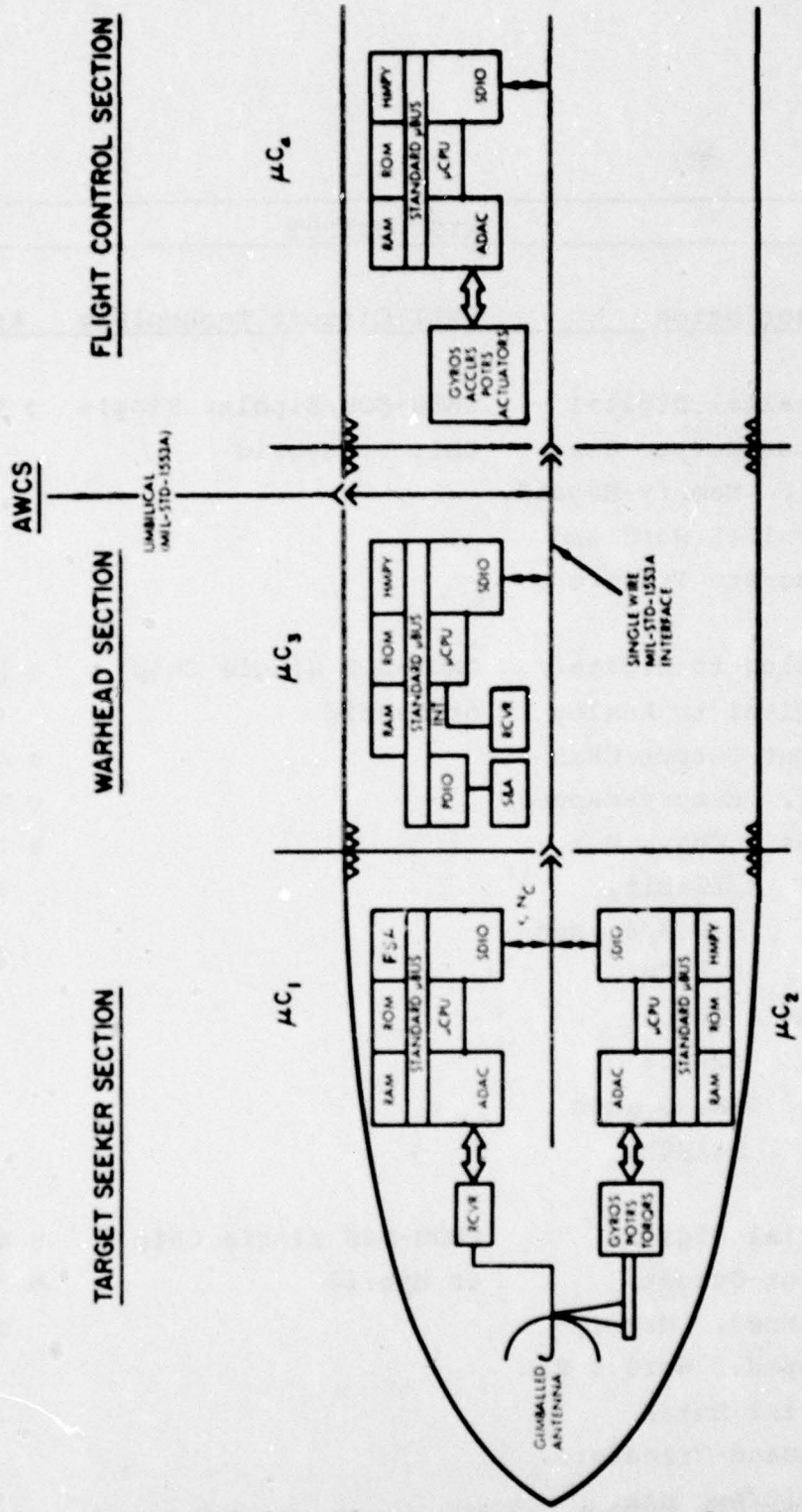

Figure 1 - Macro Modular Microcomputer System for On-Board Missile Guidance and Control

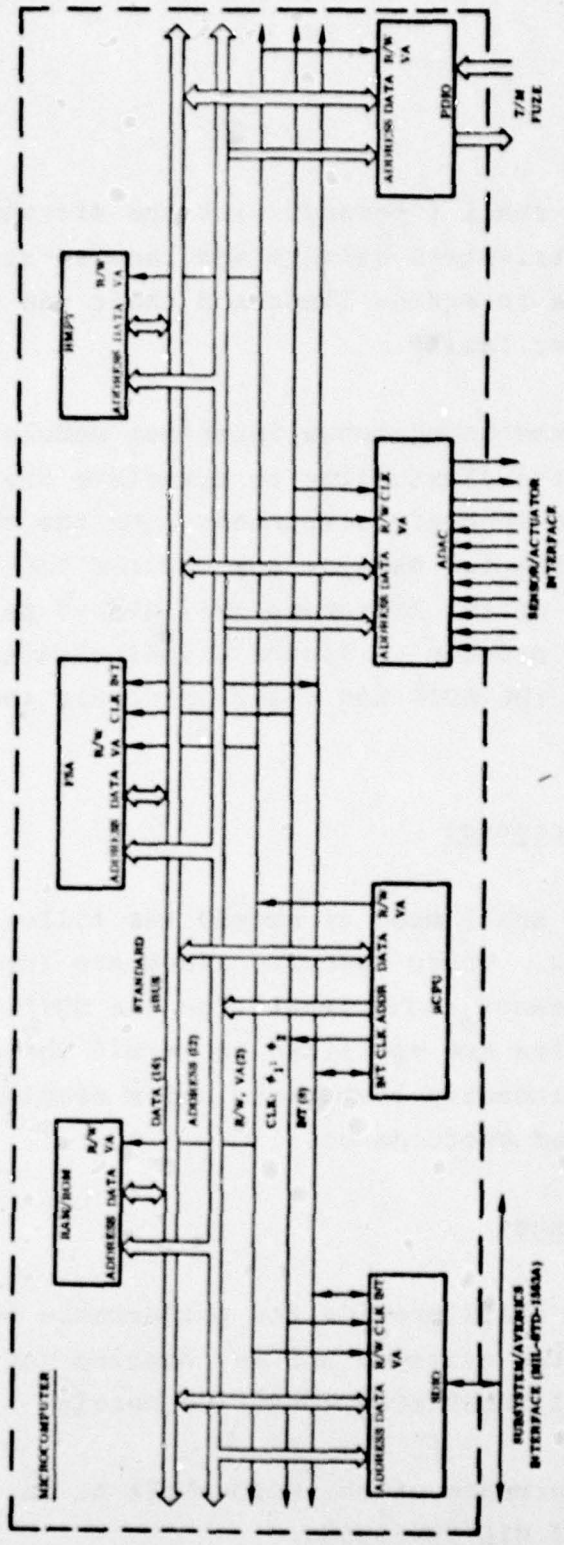

Figure 2 - Standard Microbus (μBus) Interface Lines

The SDIO shall interface with the microbus (μBus) of the microcomputer via tri-state drivers and receivers. Figure 2 shows the individual μBus interface lines and their use by other modules of the microcomputer family.

A programmable microbus interface module (MIM) shall be used: to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface; to map the two RAMs at any desired location within the total memory space of the microcomputer; and to perform the data link communication protocol. Figure 3 indicates the major functional elements of the SDIO and their interrelationship with one another.

3.2 Characteristics

The SDIO shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for the SDIO. Only the significant characteristics are specified to permit the choice of any suitable standard-industry components and a combination thereof to achieve the required performance.

3.2.1 Performance

The SDIO shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein.

The performance of the SDIO shall be in compliance with the requirements of MIL-STD-1553B.

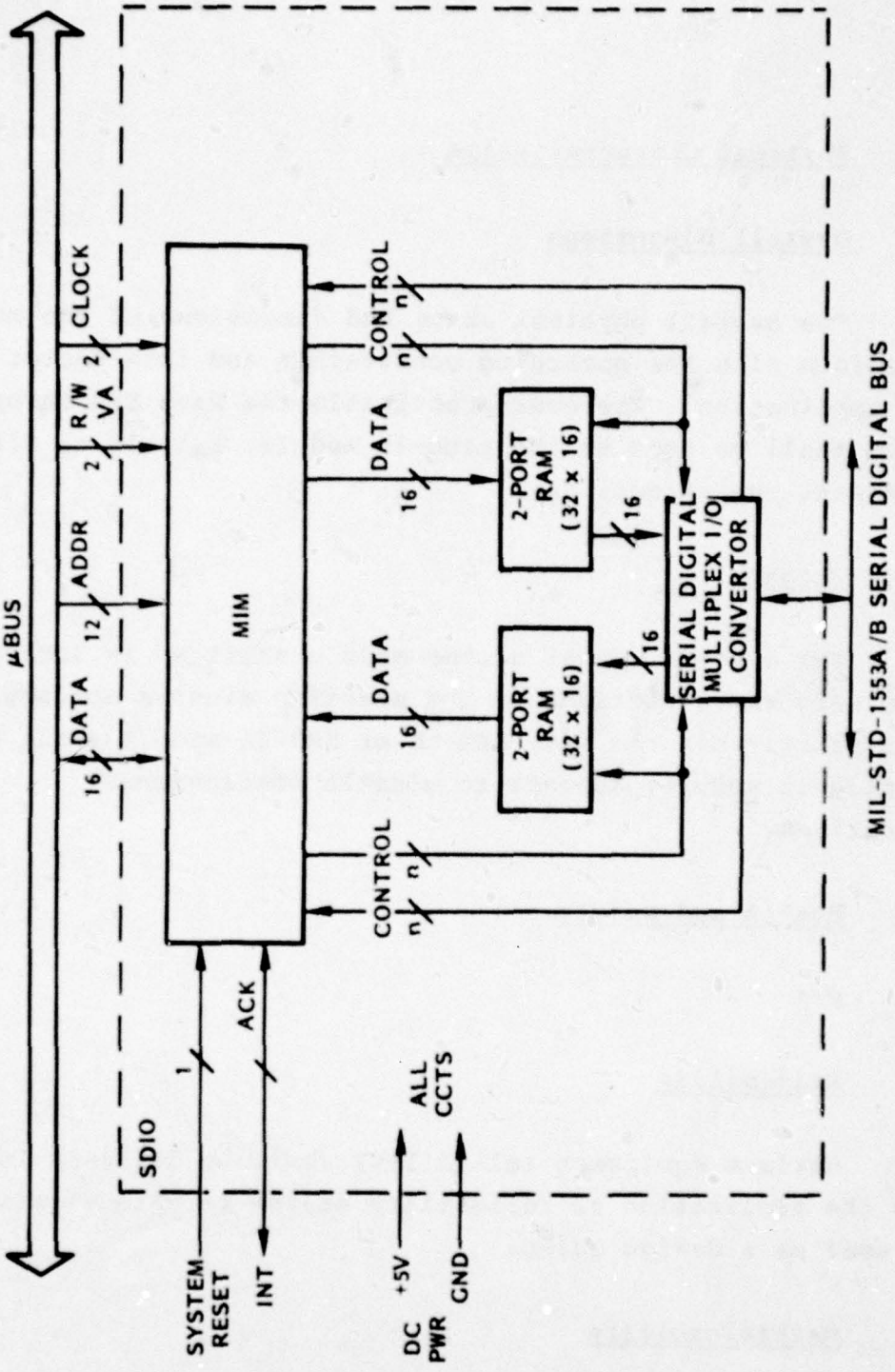

Figure 3 - General Block Diagram of the SDIO Module

3.2.2 Physical Characteristics

3.2.2.1 Overall Dimensions

The overall physical shape and dimensions of the module shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.2 Weight

The overall weight of the module shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The module shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The module shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The module shall meet the performance requirements of paragraph 3.2.1 during exposure to temperature ranging from -28°C to +71°C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over the range specified in 3.2.5.1 at a rate of change of 1° per second.

3.2.5.2 Shock

The module shall operate as specified herein after being subjected to ±15g peak shock impulse of 11 milliseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibration associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure tc a relative humidity of 95% at temperatures to +120°F.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be appropriately selected to meet the requirements of paragraph 3.2.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The module shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The module shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition, the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as applicable.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

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4.2 Quality Conformance Inspections

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5.0 PREPARATION FOR DELIVERY

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6.0 NOTES

Issue: Preliminary

CRITICAL ITEM
PRODUCT FUNCTION SPECIFICATION
FOR
PARALLEL DIGITAL
INPUT OUTPUT (PDIO)
OF THE
NAVY MACRO-MODULAR MICROCOMPUTER FAMILY

1.0 SCOPE

This specification establishes the performance, design, test, manufacture, and acceptance requirements for the Parallel Digital Input Output (PDIO) module of the Navy Macromodular Microcomputer Family hereinafter referred to as the module.

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the issue in effect on the date of invitation for bid or request for proposal form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400	Electronic Equipment Airborne General Specifications for

Standards

Military

MIL-STD-883	Test Methods and Procedures for Microelectronics

Drawings

2.2 Order of Precedence

Conflicting requirements arising between this specification, or any specification, standard drawing or publication listed herein, shall be referred in writing to the contractor for interpretation, clarification, resolution or correction. In general, documents shall rank in the following order of precedence.

a. This specification

b. All other referenced documents

3.0 REQUIREMENTS

3.1 Item Definition

The PDIO module forms one of the set of VLSIC modules in the Navy Macromodular Microcomputer Family for digital missile guidance and control applications.

Table 1 is a listing of the modules in the Family. Figure 1 shows various combinations of the modules to form complete microcomputers with varying performance capabilities in a federated microcomputer system for on-board missile guidance and control.

3.1.1 Item Diagrams

The microcomputer modules which shall interface with the PDIO via a standard microbus (μBus) are: microprocessors μCPU-1 and μCPU-2; read-write and (programmable) read-only memory (RAM/(P)ROM); analog-to-digital and digital-to-analog (ADAC) convertors; serial digital input-output (SDIO) module; high-speed frequency spectrum analyzer or fast Fourier transform module, (FSA) and a high-speed multiply module (HMPY), (Figure 2).

The PDIO module shall provide input output storage for two parallel 16-bit data words, (one input, one output respectively), as part of the memory mapped I/O scheme. As such, the PDIO appears as a two-word read/write memory on the μBus and shall have the same interface as a RAM or (P)ROM module.

TABLE 1

MICROCOMPUTER MACROMODULES

MICROPROCESSORS

Module	Description	VSLI Circuit Technology	Application
µCPU-1	Medium-Speed Microprocessor/ Central Processing Unit, 16-Bit General-Register 600 nsec R-R Add Max.	N-MOS, CPU-on a Chip,	o Telemetry o Fuzing o Head Control o Autopilot
µCPU-2	High-Speed Microprocessor/ Central Processing Unit, 16-Bit Word, Fixed-Point, General-Register, 150 nsec R-R Add Max.	CMOS-SOS, Bit-Slice RALU and µPCU Hybrids (2900/3000 Series or Equiv.) or Multi µCPU-1 Processor.	o Autopilot (Adaptive) o Signal Processing o Estimation o Guidance

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
HMPY	High Speed Multiplier, Memory-Mapped 200 nsec, Max. 16x16-bit Multiply	CMOS-SOS Single Chip or Hybrid	o Throughput Enhancement for µCPU E. G. Class I Sig. Proc.
FSA	High-Speed Frequency Spectrum Analyzer Memory-Mapped, 150 µsec Max. for 64-pts, 8 + J8. Pre-Programmable for 128, 256 or 512 pts.	CMOS-SOS or CCD FFT/CZT ALU and µPCU Hybrids (2900 Series or Equiv.)	o Throughput Enhancement for µCPUs E. G. Class II & III Sig. Proc.
RAM-1	Random-Access, Read/ Write Memory, Medium Speed, 128-2Kx16-Bits 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Data o Telemetry o Fuzing o Head Control o Autopilot
P/ROM-1	Programmable (Mask/ Electrically) Read-Only Memory, Medium Speed, 1K-16Kx16-Bits, 500 nsec Max. Access Time	N-MOS Single Chip or Hybrid	Programs

HIGH-SPEED ARITHMETIC AND MEMORIES

Module	Description	VSLI Circuit Technology	Application
RAM-2	Random-Access, Read/ Write Memory, High-Speed 256-1Kx16-bits 100 nsec Max. Access Time	CMOS-SOS Single Chip or Hybrid	Data o Sig. Proc. o Estimation o Guidance o Head Control o Autopilot o Fuzing
P/ROM-2	Programmable (Mask/ Electrically) Read-Only Memory, High-Speed, 1K-4Kx16-bits 100 nsec Max. Access Time	CMOS/SOS Single Chip or Hybrid	Programs

INPUT-OUTPUT

Module	Description	VSLI Circuit Technology	Application
PDIO	Parallel Digital Input-Output Channel. Memory-Mapped. Parallel Word and Discrete Transfers	CMOS-SOS/Bipolar Single Chip or Hybrid	o Telemetry
ADAC	Analog to Digital/ Digital to Analog Input-Output Channel. Memory-Mapped. A-D: 8 Chs., Mux. 8/12-Bit, A-D 3/8 μsec Max/Ch. D-A: 4 Chs., 12-bit D-A, 5 μsec Max/Ch.	CMOS-SOS Single Chip or Hybrid	o Head Control o Autopilot o Telemetry o Radar Receiver
SDIO	Serial Digital Input-Output Channel. Memory-Mapped. Word & Bit Serial Data/ Command Transfers, 1Mbit/sec Max. MIL-STD-1553A/B	CMOS-SOS Single Chip or Hybrid	o Avionics o Inter Microcomputer

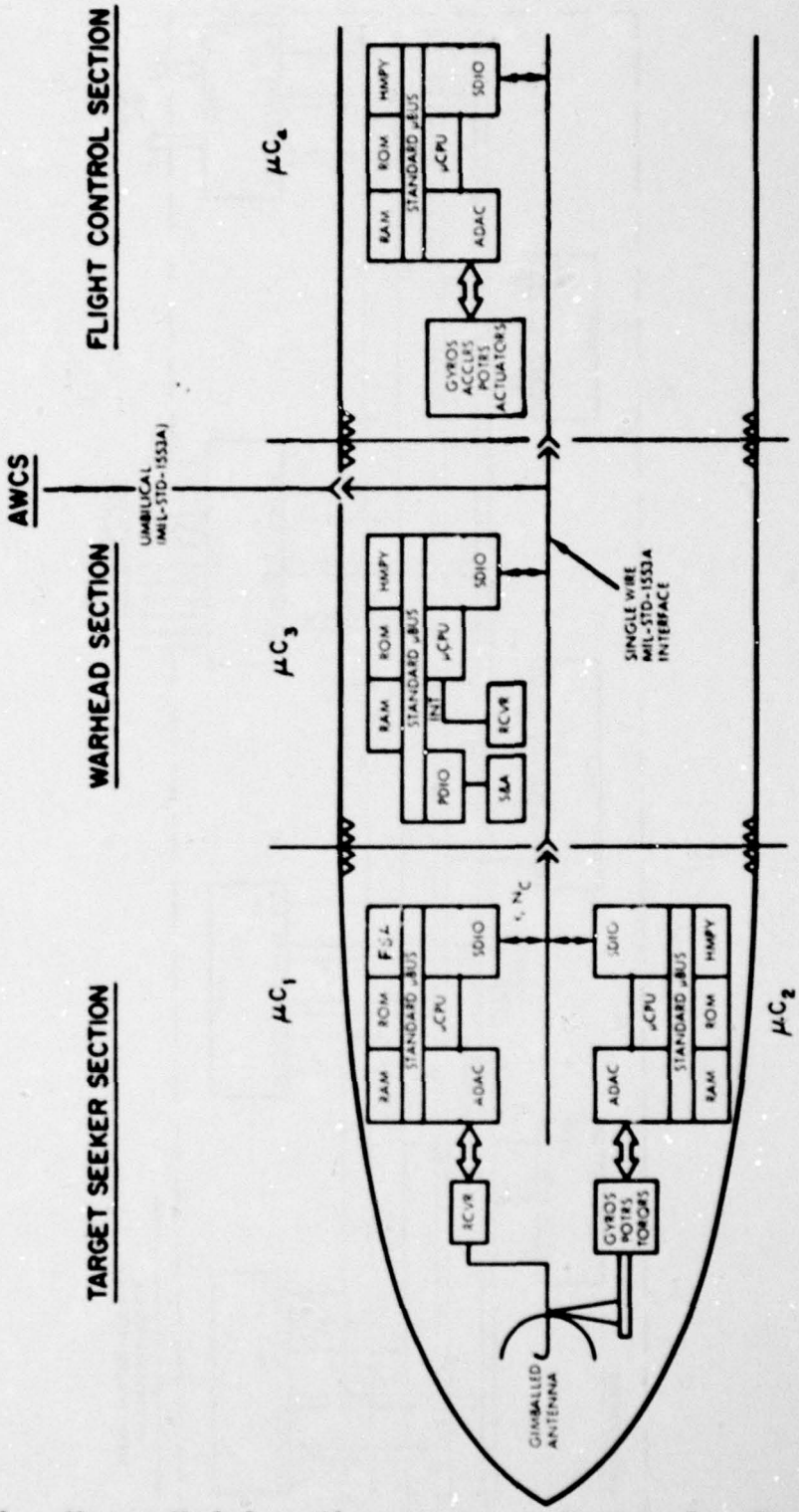

Figure 1 - Macro-Modular Microcomputer System for On-Board Missile Guidance and Control

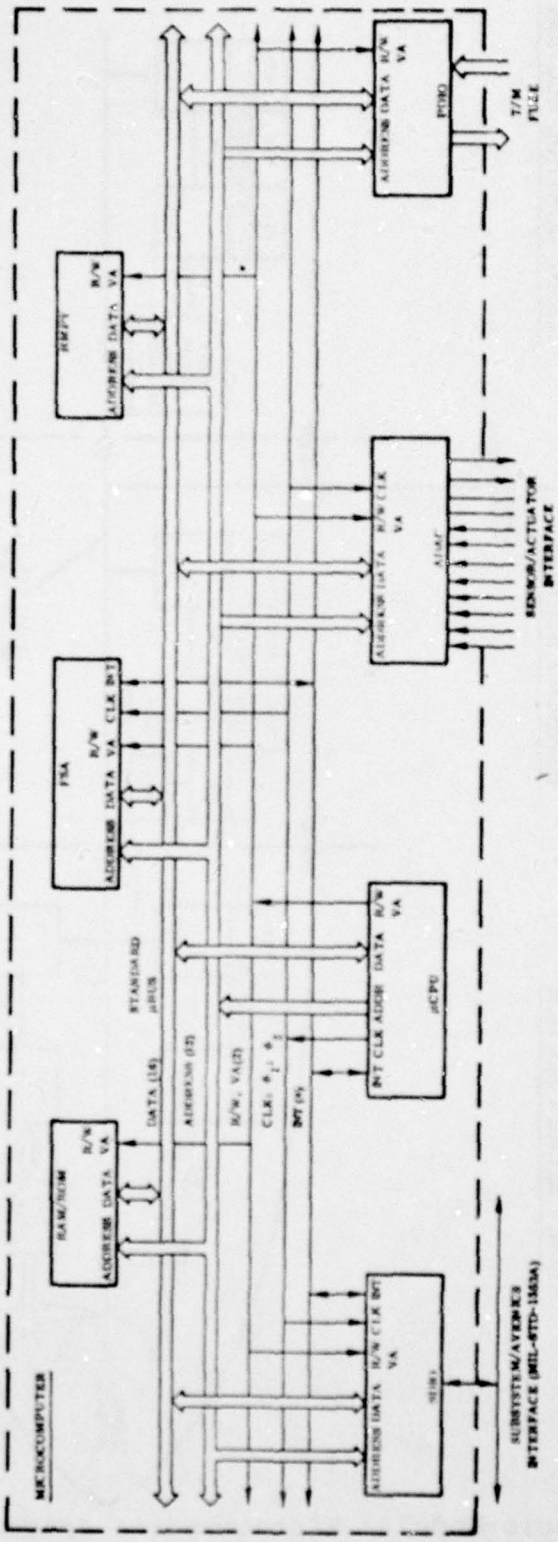

Figure 2 - Standard Microbus (μBus) Interface Lines

The PDIO shall interface with the microbus (μBus) of the microcomputer via tri-state drivers and receivers. Figure 2 shows the individual μBus interface lines and their use by the memory and input-output interface modules of the microcomputer.

A microbus interface module (MIM) shall be used to provide the flexibility to translate the interface lines of various standard-industry components into the common microbus interface, and to provide programmable mapping of the two registers in any location within the total memory map/space of the microcomputer.

On the system side of the module, 16 discrete output lines and 16 discrete input lines shall be provided for use as either whole computer word or digital discrete I/O. The latter I/O interface shall be at transistor-transistor logic (T^2L) levels with the capability to drive one input and load not less than one T^2L gate at the output.

Figure 3 indicates the major functional elements of the PDIO module and their interrelationship with one another.

3.2 Characteristics

The PDIO module shall meet or exceed the following major functional requirements. These specifications are intended to satisfy the minimum performance requirements for the PDIO. Only the significant characteristics are specified to permit the choice of any suitable standard-industry components and combination of thereof to achieve the required performance.

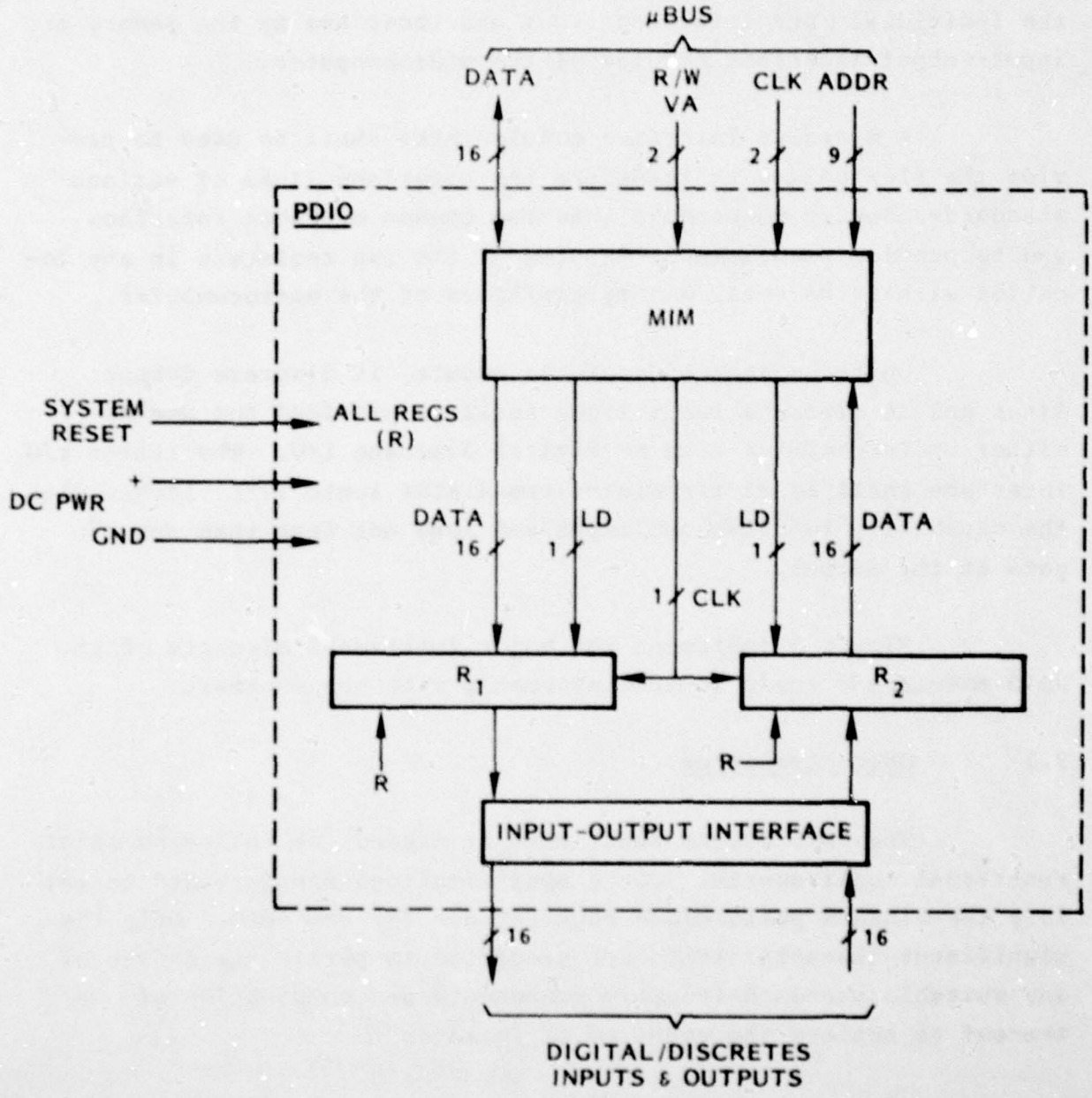

Figure 3 - General Block Diagram of Parallel Digital Input-Ouput Module

3.2.1 Performance

The PDIO shall provide the performance specified herein when subjected to the extremes and any combination of the functional and physical interfaces specified herein.

3.2.1.1 Cycle Time

The PDIO read/write cycle time shall be 100 nsecs max.

3.2.2 Physical Characteristics

3.2.2.1 Overall Dimensions

The overall physical shape and dimensions of the module shall conform with the packaging constraints and form factor of the missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.2 Weight

The overall weight of the module shall be in accordance with the weight restrictions of the specific missile application. Wherever practicable the Navy SEM-1A or SEM-2A module shall be used as the plug-in module, subject to missile environmental qualifications.

3.2.2.3 Health and Safety

N/A

3.2.3 Reliability

Maximum equipment reliability shall be designed in through the application of reliability design techniques with MIL-E-5400 used as a design guide.

3.2.4 Maintainability

The module shall be designed to be repairable at an appropriately equipped facility.

3.2.5 Environmental Requirements

The module shall meet all the requirements specified herein during and after exposure to any or all the environments specified below.

3.2.5.1 Temperature

The module shall meet the performance requirement of paragraph 3.2.1 during exposure to temperatures ranging from -28°C to +71°C.

3.2.5.1.1 Nonoperating Storage Temperature

The module shall withstand exposures to temperatures ranging from -62°C to +71°C.

3.2.5.1.2 Thermal Shock

The module shall operate as specified herein when the temperature varies over the range specified in 3.2.5.1 at a rate of change of 1^{o} per second.

3.2.5.2 Shock

The module shall operate as specified herein after being subjected to ±15g peak shock impulse of 11 missiseconds duration along 3 mutually perpendicular axes.

3.2.5.3 Acceleration

The module shall operate as specified herein while being subjected to the linear acceleration of 17gs in any direction.

3.2.5.4 Vibration

The module shall operate as specified herein when subjected to vibrations associated with missile launch effects.

3.2.5.5 Altitude

The module shall operate at altitudes from sea level to 70,000 feet.

3.2.5.6 Humidity

The module shall be capable of meeting the performance requirements specified in paragraph 3.2.1 during and after exposure to a relative humidity of 95% at temperatures to $+120^{o}F$.

3.2.6 Transportability

The module shall be transportable by highway, rail or air when properly packaged.

3.3 Design and Construction

The design and construction requirements contained herein are considered a minimum standard and shall ensure that all requirements in this specification can be met.

3.3.1 Materials Processes and Parts

Parts, materials and processes shall be appropriately selected to meet the requirements of paragraph 3.2.

3.3.2 Electromagnetic Radiation

3.3.2.1 Electromagnetic Interference (EMI)

The module shall be designed to meet the appropriate EMI requirements specified in MIL-STD-461.

3.3.3 Identification and Marking

The module shall be legibly and permanently marked in accordance with MIL-STD-130.

3.3.4 Workmanship

All details of workmanship shall be of the highest grade consistent with the intention of this specification. In addition,

the equipment shall be constructed in accordance with Requirements 5 and 9 of MIL-STD-454, as applicable.

3.3.5 Interchangeability

All modules manufactured to this specification shall be electrically and mechanically interchangeable.

3.3.6 Safety

The optimum degree of safety within the constraints of operational effectiveness, time and cost shall be attained through the application of safety principles in accordance with MIL-S-38130.

3.3.7 Human Performance/Human Engineering

All test points and electrical connectors shall be permanently labeled to provide clearest description in terms of legibility and identification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

Test examinations and inspections shall be performed on the module to verify that the requirements of Section 3 have been met.

4.1.1 Responsibility for Inspection

Unless otherwise specified, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may use his own or any facilities suitable for the performance of the test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform and/or witness any of the tests set forth in this document where such tests are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.2 Special Tests and Examinations

TBDL

4.2 Quality Conformance Inspections

TBDL

5.0 PREPARATION FOR DELIVERY

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